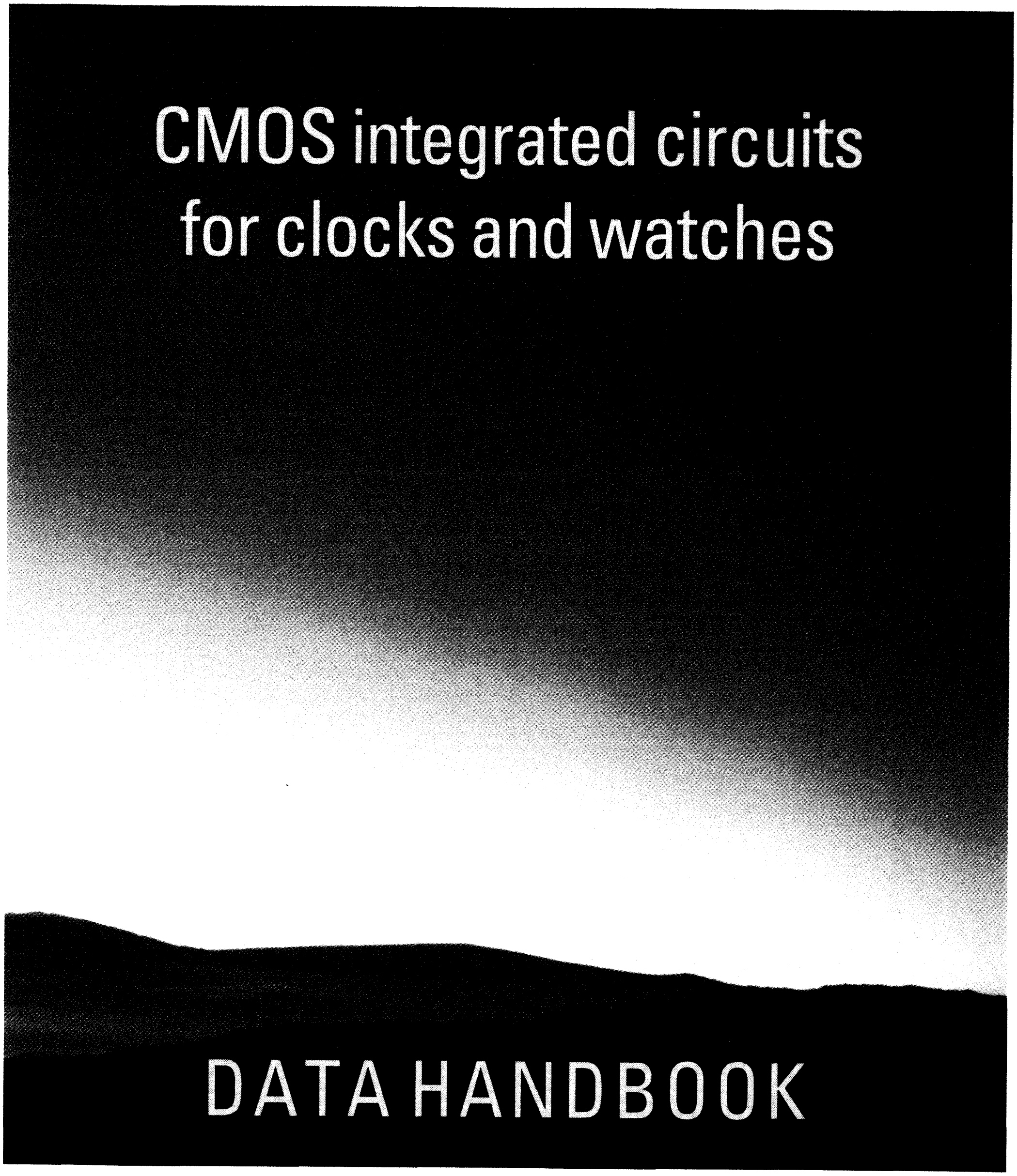
INTEGRATED CIRCUITS



CMOS integrated circuits for clocks and watches

DATA HANDBOOK

BOOK IC16 1994

Philips Semiconductors

PHILIPS

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

CMOS Integrated Circuits for Clocks and Watches

CONTENTS

INTRODUCTION

CMOS integrated circuits for clocks and watches

Introduction

Faselec, a Philips IC subsidiary, is one of the most important producers of CMOS integrated circuits for clocks and watches in the world. Situated in Switzerland, the heart of the European clock and watch industry, Faselec benefits to a large degree from this unique industrial environment. It is therefore not surprising, that Faselec was one of the first semiconductor companies to apply the silicon gate CMOS (complementary metal oxide semiconductor) technology in the production of clock and watch circuits and was the first company to offer an SO-package (mini-pack) back in the seventies.

Faselec maintains its position at the forefront of the clock and watch IC industry, being the first company to offer the EEPROMs (Electrically Erasable Programmable Read Only Memories), with operating voltages as low as 1.1 V, for time adjustment. This latest development enables the industry to find better technical and cost effective solutions for their products.

To enable the clock and watch industry to maintain its world-renowned quality image, Faselec has implemented a Company-Wide Total Quality Management (TQM) program. This TQM program, involving every employee of Faselec, features a continuous improvement of customer service and product quality. This commitment to quality has lead to us being able to set our standard at zero defects and now enables us to offer our customers a zero defects warranty. The warranty means that if he finds a single device which does not conform to the published specification, the customer can return the complete lot for rescreening or replacement. Faselec is the first company in the world to offer the clock and watch industry a zero defects warranty.

At Faselec quality dominates all phases of manufacture. Quality is built into the product by the conscious use of advanced technological aids and a continuous monitoring of all process steps (SPC) through in-line quality controls. Additionally a stringent incoming inspection of all materials used assures an end-product with an inherently high quality level.

All products are 100% tested against published specifications, any device not conforming to the specifications is rejected. Conformity of each lot to the published specifications is double-checked by our Quality department, which is independent from production.

The dedication of the high-qualified personnel and the large amount of know-how accumulated over the years, backed by constant efforts in developing new process and packaging technology as well as new products, makes Faselec the preferred source for your clock and watch circuits.

DEFINITIONS AND STATEMENTS

DEFINITIONS AND STATEMENTS

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

SELECTION GUIDE

Analog watch circuits: 32 kHz

Table 1 Watch circuit overview PCA146X.

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS						PAGE
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	
PCA1461	U	1	7.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	35
PCA1462	U	1	5.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	35
PCA1463	U	1	3.9	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	35
PCA1464	U/10	0.5	3.9	81	P = 1 N = 2	no	no	no oscillator 3.0 V Lithium	35
PCA1465	U/10; U/7	1	5.8	max. 100	P = 1 N = 2	yes	no	1.5 V	35
PCA1466	T	5	5.8	max. 100 81	P = 1 N = 2	no	no	1.5 V and 2.1 V Lithium	35
PCA1467	U/10	1	7.8	100	P = 1 N = 2	yes	no		35

Table 2 Watch circuit overview PCA148X.

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS						PAGE
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	
PCA1482	U; U/7; T	1	5.8	75	P = 2 N = 3	yes	yes		51
PCA1483	U/7	1	5.8	75	P = 2 N = 3	yes	no		51
PCA1484	U/7	20	5.8	75	P = 2 N = 3	yes	no	C_i = 8 pF 2.1 V C_o = 12 pF	51
PCA1485	U/7	1	5.8	75	P = 1 N = 2	yes	yes		51
PCA1486	U/7	1	5.8	75	P = 1 N = 2	yes	no		51
PCA1487	U/5; T	1	7.8	75	P = 2 N = 3	yes	yes		51

Table 3 Watch circuit overview PCA16XX.

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS					PAGE
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS	
PCA1602	T	1	7.8	75	yes	no		76
PCA1603	U/7	20	7.8	100	yes	no		76
PCA1604	U; T	5	7.8	75	yes	no		76
PCA1605	U/7	5	4.8	75	yes	no		76
PCA1606	U/10	10	6.8	100	yes	no		76
PCA1607	U	5	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium	76
PCA1608	U	5	7.8	100 75	yes	no	1.5 V and 2.1 V Lithium	76
PCA1611	U	1	6.8	75	yes	no		76
PCA1624	U	12	3.9	75 56	yes	no	1.5 V and 2.1 V Lithium	76
PCA1625	U/7	5	5.8	75	yes	no		76
PCA1626	U	20	5.8	100	yes	no		76
PCA1627	U/7	20	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium	76
PCA1628	U	20	5.8	75	yes	no		76
PCA1629	U/7	5	6.8	75	yes	no		76

Table 4 Watch circuit overview PCA167X (3 V lithium).

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS					PAGE
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS	
PCA1672	T	1	7.8	56	no	no	3 V Lithium	85
PCA1673	U	1	5.8	56	no	no	3 V Lithium	85
PCA1675	U	1/16	5.8	100	no	no	no oscillator	85
PCA1676	U/10	10	5.8	56	no	no	3 V Lithium	85
PCA1677	T	10	7.8	100	no	no	1.5 V	85

Notes to Tables 1 to 4

U = Chip in trays.

U/5 = Wafer.

U/7 = Chip with bumps on tape.

U/10 = Chip on foil.

Analog alarm clock circuits: 32 kHz quartz crystal

Table 5 Alarm clock circuit overview PCA159X.

TYPE NUMBER	OUTPUT CYCLE TIME (ms)	PULSE WIDTH t_p (ms)	CURRENT CONSUMPTION (μA)		EEPROM	REMARKS	PAGE
			TYP.	MAX.			
PCA1593	1	31.25	1.5	5	yes	PCA159X series have: EEPROM for frequency trimming; 64 steps 2 kHz alarm output; alarm output of PCA1593, PCA1594 and PCA1596 is shown in Fig.1 (Alarm Signal A); alarm output of PCA1595 and PCA1597 is shown in Fig.1 (Alarm Signal B)	65
PCA1594	1	46.8	1.5	5	yes		65
PCA1595	1	46.8	1.5	5	yes		65
PCA1596	1	15.6	1.5	5	yes		65
PCA1597	4	15.6	1.5	5	yes		65

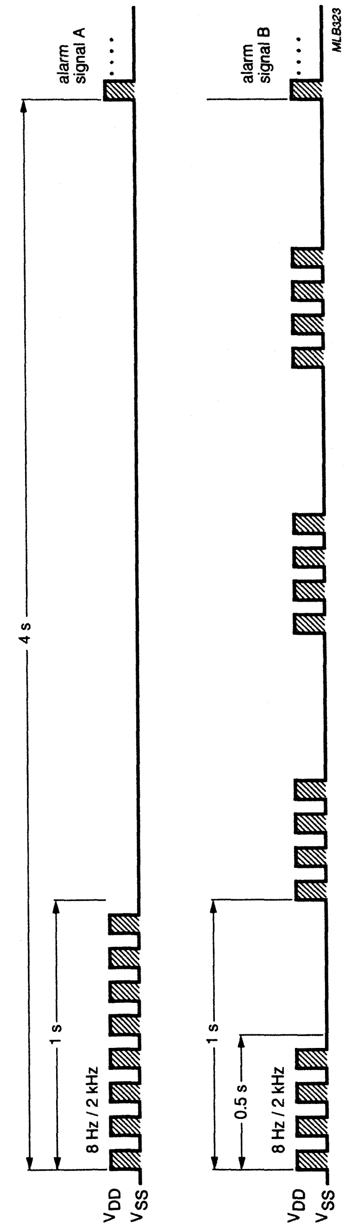


Fig.1 Alarm output waveforms.

Digital car clock circuits: 4.19 MHz quartz crystal

Table 6 Car clock circuit overview PCF1171C to PCF1179C.

TYPE NUMBER	DIGITS	FUNCTIONS									TYPICAL SUPPLY CURRENT (μA)	REMARKS	PAGE
		A	B	C	D	E	F	G	H	I			
PCF1171C	4.0	•	•		•	•	•		•		400		90
PCF1172C	3.5	•		•	•	•	•		•		400		98
PCF1174C	4.0	•	•	•	•	•	•		•	•	950	note 1	106
PCF1175C	4.0	•	•	•	•	•		•	•	•	950	note 1	118
PCF1178C	4.0	•	•	•	•	•		•	•	•	950	note 1	130
PCF1179C	4.0	•	•	•	•	•		•	•	•	950	note 1	142

Note

1. EEPROM for time calibration and voltage regulation for LCD.

Where columns A to I are the functions for:

A = 12 hour mode.
B = 24 hour mode.
C = AM/PM annunciator.
D = hours.
E = minutes.
F = direct drive.
G = duplex drive.
H = internal voltage regulator.
I = EEPROM.

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	PAGE
PCA1461	U	1	7.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	35
PCA1462	U	1	5.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	35
PCA1463	U	1	3.9	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	35
PCA1464	U/10	0.5	3.9	81	P = 1 N = 2	no	no	no oscillator 3.0 V Lithium	35
PCA1465	U/10; U/7	1	5.8	max. 100	P = 1 N = 2	yes	no	1.5 V	35
PCA1466	T	5	5.8	max. 100 81	P = 1 N = 2	no	no	1.5 V and 2.1 V Lithium	35
PCA1467	U/10	1	7.8	100	P = 1 N = 2	yes	no		35
PCA1482	U; U/7; T	1	5.8	75	P = 2 N = 3	yes	yes		51
PCA1483	U/7	1	5.8	75	P = 2 N = 3	yes	no		51
PCA1484	U/7	20	5.8	75	P = 2 N = 3	yes	no	C_i = 8 pF 2.1 V C_o = 12 pF	51
PCA1485	U/7	1	5.8	75	P = 1 N = 2	yes	yes		51
PCA1486	U/7	1	5.8	75	P = 1 N = 2	yes	no		51
PCA1487	U/5; T	1	7.8	75	P = 2 N = 3	yes	yes		51

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS						PAGE
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	
PCA1593	32 kHz alarm car clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 1 s; t_T = 1 s; t_P = 31.25 ms								65
PCA1594	32 kHz alarm car clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 4 s; t_T = 1 s; t_P = 46.8 ms								65
PCA1595	32 kHz alarm car clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 1 s; t_T = 1 s; t_P = 46.8 ms								65
PCA1596	32 kHz alarm car clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 4 s; t_T = 1 s; t_P = 15.6 ms								65
PCA1597	32 kHz alarm car clock circuit with frequency adjustment; EEPROM; bipolar motor; alarm signal repeated every 1 s; t_T = 4 s; t_P = 15.6 ms								65

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS						PAGE
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	
PCA1602	T	1	7.8	75		yes	no		76
PCA1603	U/7	20	7.8	100		yes	no		76
PCA1604	U; T	5	7.8	75		yes	no		76
PCA1605	U/7	5	4.8	75		yes	no		76
PCA1606	U/10	10	6.8	100		yes	no		76
PCA1607	U	5	5.8	100 75		yes	no	1.5 V and 2.1 V Lithium	76
PCA1608	U	5	7.8	100 75		yes	no	1.5 V and 2.1 V Lithium	76
PCA1611	U	1	6.8	75		yes	no		76
PCA1624	U	12	3.9	75 56		yes	no	1.5 V and 2.1 V Lithium	76
PCA1625	U/7	5	5.8	75		yes	no		76
PCA1626	U	20	5.8	100		yes	no		76
PCA1627	U/7	20	5.8	100 75		yes	no	1.5 V and 2.1 V Lithium	76
PCA1628	U	20	5.8	75		yes	no		76
PCA1629	U/7	5	6.8	75		yes	no		76

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS						PAGE
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	
PCA1672	T	1	7.8	56		no	no	3 V Lithium	85
PCA1673	U	1	5.8	56		no	no	3 V Lithium	85
PCA1675	U	1/16	5.8	100		no	no	no oscillator	85
PCA1676	U/10	10	5.8	56		no	no	3 V Lithium	85
PCA1677	T	10	7.8	100		no	no	1.5 V	85
PCF1171C	4.19 MHz digital LCD car clock; 4 digits								90
PCF1172C	4.19 MHz digital LCD car clock; 3½ digits								98
PCF1174C	4.19 MHz 4-digit static LCD car clock; EEPROM								106
PCF1175C	4.19 MHz 4-digit duplex CD car clock; EEPROM								118
PCF1178C	4.19 MHz 4-digit duplex LCD car clock; EEPROM; mirrored version of PCF1175; different colon and set frequency								130
PCF1179C	4.19 MHz 4-digit duplex LCD car clock; EEPROM								142

Notes

U = Chip in trays.

U/5 = Wafer.

U/7 = Chip with bumps on tape.

U/10 = Chip on foil.

T = SOT144.

CMOS integrated circuits for clocks and watches

Maintenance type list

The types listed below are not included in this handbook. Detailed information will be supplied on request.

- PCA1200 series (superseded by PCA167X series)
- PCA1400 series (superseded by PCA16XX series)
- PCA1512
- PCA1517
- PCA153X series
- PCA1580 series
- PCF1171 series (superseded by PCF1171C)
- PCF1172 series (superseded by PCF1172C)
- PCF1174 series (superseded by PCF1174C)
- PCF1175 series (superseded by PCF1175C)

GENERAL

QUALITY

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

QUALITY ASSURANCE

Based on ISO 9000 standards, customer standards such as Ford Q1 and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates.

PARTNERSHIPS WITH CUSTOMERS

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes.

PARTNERSHIPS WITH SUPPLIERS

Ship-to-stock, statistical process control and ISO 9000 audits.

QUALITY IMPROVEMENT PROGRAMME

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- Periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S	solitary digital circuits
T	analog circuits
U	mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA	microcomputer or central processing unit
MB	slice processor (functional slice of microprocessor)
MD	related memories
ME	other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH	hybrid circuits
NL	logic circuits
NM	memories
NS	analog signal processing using switched capacitors
NT	analog signal processing using charge-transfer devices
NX	imaging devices
NY	other related circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A	temperature range not specified below
B	0 to + 70 °C
C	−55 to +125 °C
D	−25 to + 70 °C
E	−25 to + 85 °C
F	−40 to + 85 °C
G	−55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C	cylindrical
D	ceramic dual in-line (CERDIL, CERDIP)
F	flat pack (two leads)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

G flat pack (four leads)
H quad flat pack (QFP)
L chip on tape (foil)
P plastic dual in-line (DIL)
Q quad in-line (QUIL)
T mini pack (SOL, SO, VSO)
U uncased chip

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C cylindrical
D dual in-line (DIL)
E power DIL (with external heatsink)
F flat pack (leads on two sides)
G flat pack (leads on four sides)
H quad flat pack (QFP)
K diamond (TO-3 family)
M multiple in-line (except dual, triple and quad)
Q quad in-line (QUIL)
R power QUIL (with external heatsink)
S single in-line (SIL)
T triple in-line
W leaded chip carrier (LCC)
X leadless chip carrier (LLCC)
Y pin grid array (PGA)

SECOND LETTER (MATERIAL)

C metal-ceramic
G glass-ceramic
M metal
P plastic

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

Assembly

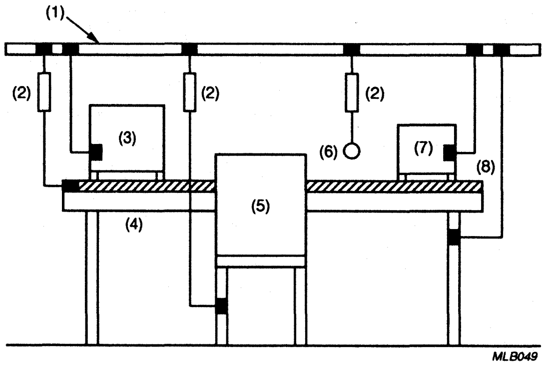
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.

(2) Resistor (500 kΩ ± 10%, 0.5 W).

(3) Ionizer.

(4) Work bench.

(5) Chair.

(6) Wrist strap.

(7) Electrical equipment.

(8) Conductive surface/antistatic sheet.

Fig.1 Protected work station.

DEVICE DATA
in alphanumeric sequence

32 kHz watch circuit with adaptive motor pulse

PCA146X series

FEATURES

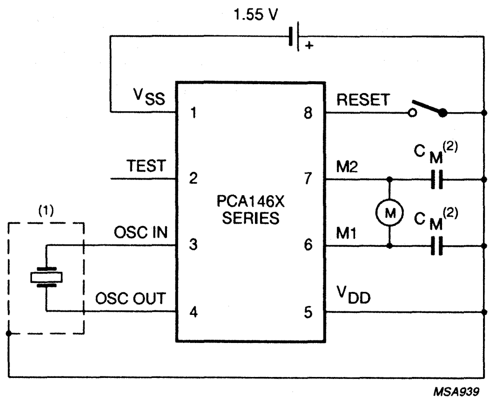
- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Time keeping adjustment electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption; typically 170 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current compared with conventional circuits, by self adaption of the motor pulse width in accordance with the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Detector for lithium or silver-oxide battery voltage levels
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA146X series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA146XT	8	micro-flat-pack	plastic	SOT144A
PCA146XU	–	chip in tray	–	–



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} or V_{SS} should be less than C_M = 80 pF for correct operation of the detection circuit. Driving the motor at its minimum energy, probe and stray capacitance must be avoided.

Fig.1 Typical application circuit diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

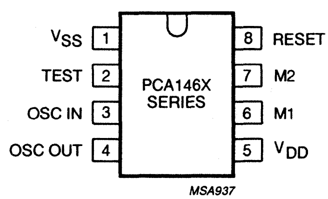


Fig.2 Pin configuration.

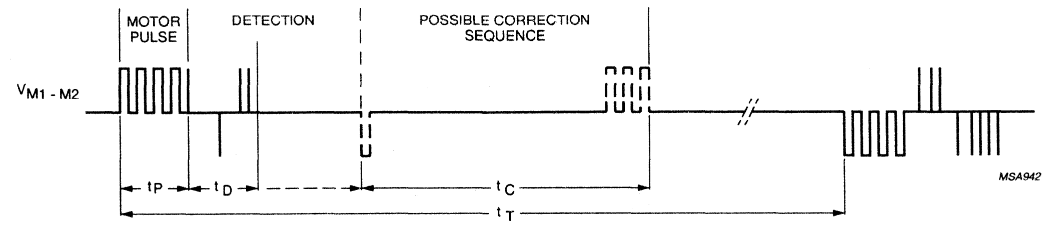


Fig.3 Possible motor output waveform in normal operation with motor connected.

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different stages depending on the torque required to turn the motor (Fig.4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. When a step is missed a correction sequence will be started (Fig.3).

Motor pulses

The circuit produces motor pulses of six different stages (stage 1 to 5, stage 8). Each stage has two independent modes; silver-oxide and lithium. The voltage level of V_{DD} determines which mode is selected (see section 'Voltage level detector').

Stages 1 to 5 (both modes) are used in normal operation, stage 8 occurs under the following conditions:

- correction pulse after a missing step (both modes)
- end-of-life mode
- if stage 5 is not enough to turn the motor (both modes).

In the silver-oxide mode, the ON state of the motor pulse varies between 56.25% and 100% of the duty factor t_{DF} = 977 µs depending on the stage (Fig.4). It increases in steps of 6.25% per stage.

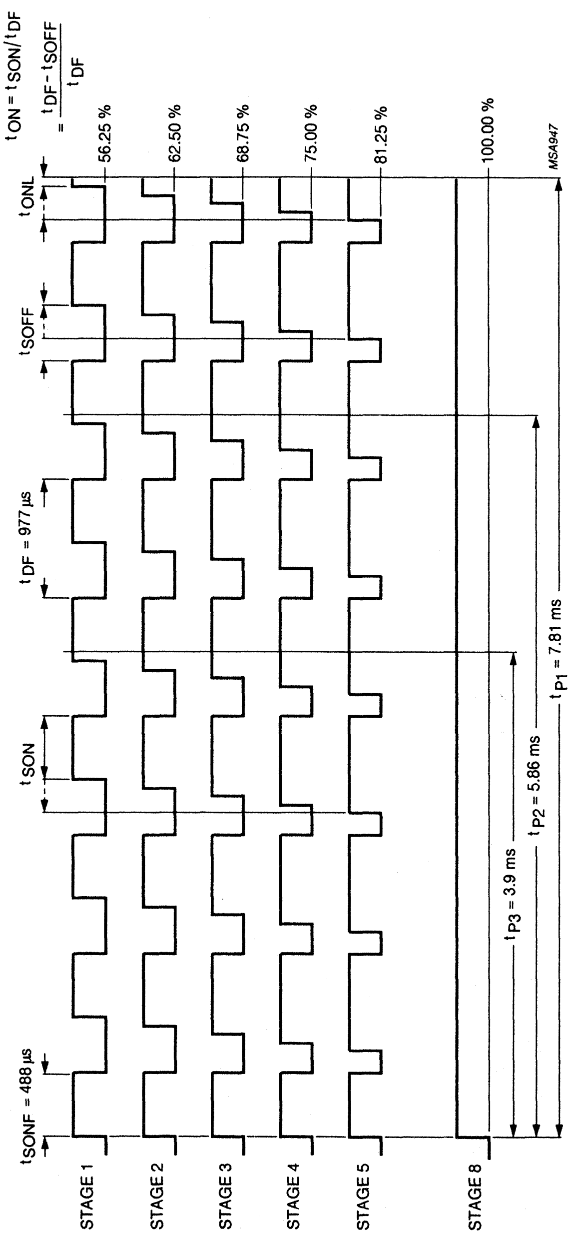
In the lithium mode, the ON state of the motor pulse is reduced by 18.75% of the duty factor t_{DF} (Fig.5) to compensate for the increase in the voltage level.

After a RESET the circuit always starts and continues with stage 1, when all motor pulses have been executed. A failure to execute all motor pulses results in the circuit going into stage 2, this sequence will be repeated through to stage 8.

When the motor pulses at stage 5 are not large enough to turn the motor, stage 8 is implemented for a maximum of 8 minutes [1] with no attempt to keep current consumption low. After stage 8 has been executed the procedure is repeated from RESET.

The circuit operates for 8 minutes[1] at a fixed stage, if every motor pulse is executed. The next 480 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and for a maximum of 8 minutes[1] the motor pulses are increased by one stage.

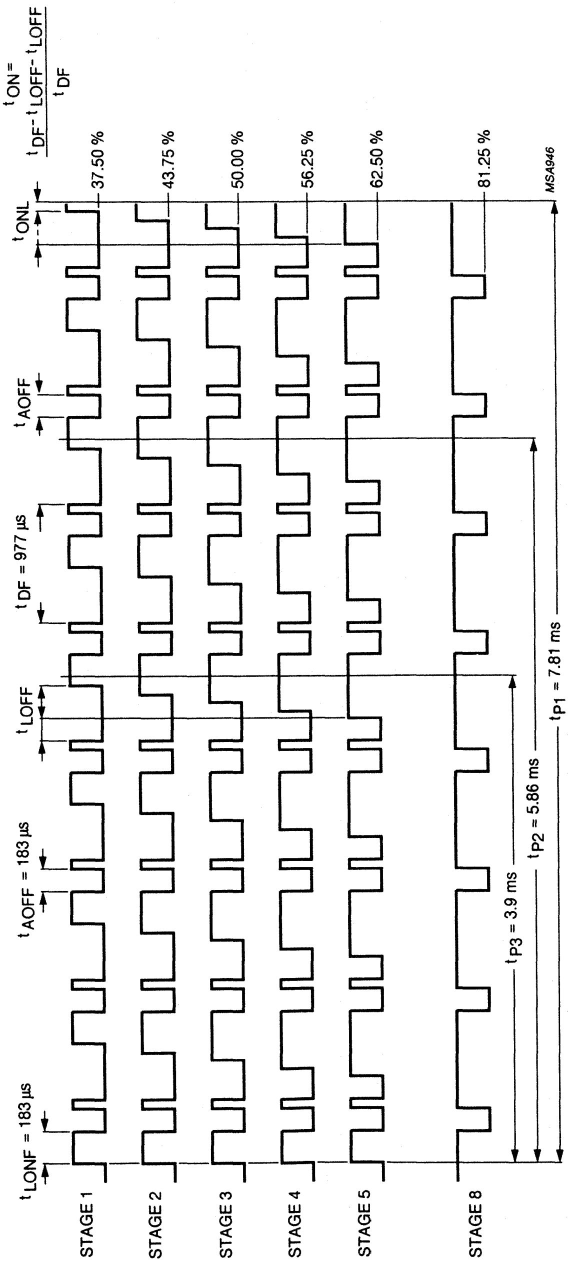
(1) 4 minutes for PCA1464.



t_{OFF} for stage 1 to 5 = 488 µs – stage x 61 µs

t_{ON} for stage 1 to 5 = 488 µs + stage x 61 µs

Fig.4 Motor pulses in the silver-oxide mode (V_{DD} = 1.55 V).



t_{OFF} for stage 1 to 5 = 672 µs – stage x 61 µs

t_{ON} for stage 1 to 5 = 305 µs + stage x 61 µs

Fig.5 Motor pulses in the lithium mode (V_{DD} = 2.1 V).

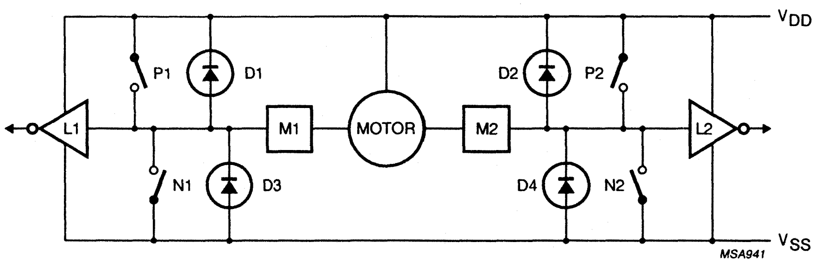


Fig.6 Motor driving and detecting circuit.

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{LIT} and V_{EOL} every minute. The first voltage level detection is carried out 30 ms after RESET.

When a lithium voltage level is detected ($V_{DD} \geq V_{LIT}$), the circuit starts operating in the lithium mode (Fig.5).

When the detected V_{DD} voltage level is between V_{LIT} and V_{EOL}, the circuit operates in the silver-oxide mode (Fig.4).

If the battery end-of-life is detected ($V_{DD} < V_{EOL}$), the detection and stage control is switched OFF and the waveform produced is an unchopped version of the stage 8 waveform. To indicate this condition the waveform is produced in bursts of 4 pulses every 4 s.

Detection of motor movement

After a motor pulse, the motor is short-circuited to V_{DD} for 1 ms. Afterwards the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig.6 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1. Then the first of 52 possible measurement cycles (t_{MC}) starts to measure the induced current.

Detection criterion (Figs 7 and 8)

Part 1

- P = 2 number of measured positive current polarities after t_{DI}.

Part 2

- N = 3 number of measured positive current polarities since the first negative current polarity is detected after part 1 (see Fig.7).

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

Correction sequence

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 29.30 ms a pulse of stage 8 (t_{C2}) to turn the motor.

Every measurement cycle (t_{MC}) has 4 phases. They are as follows:

SYMBOL	PHASE	DESCRIPTION
t_{M1}	1	During T_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.
t_{M2}	2	Measures the induced current; during a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is short-circuited to V_{DD}. Depending on the direction of the interrupted current: - the current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2; - the current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1. A succesfully detected current polarity is normally characterized by a short pulse of 0.5 to 10 µs with a voltage up to ±2.1 V, failed polarity detection by the maximum pulse width of 61 µs and a voltage of ±0.5 V (see Fig.8).
t_{M3}	3	The switches P1 and P2 remain closed for the time t_{M3}.
t_{M4}	4	If the circuit detects less pulses than P and N respectively, a pulse of the time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed. Otherwise P1 and P2 remain closed.

Detection and pulse width control will be switched OFF, when the battery voltage is below the end-of-life voltage (V_{EOL}) or if stage 5 is not sufficient to turn the motor.

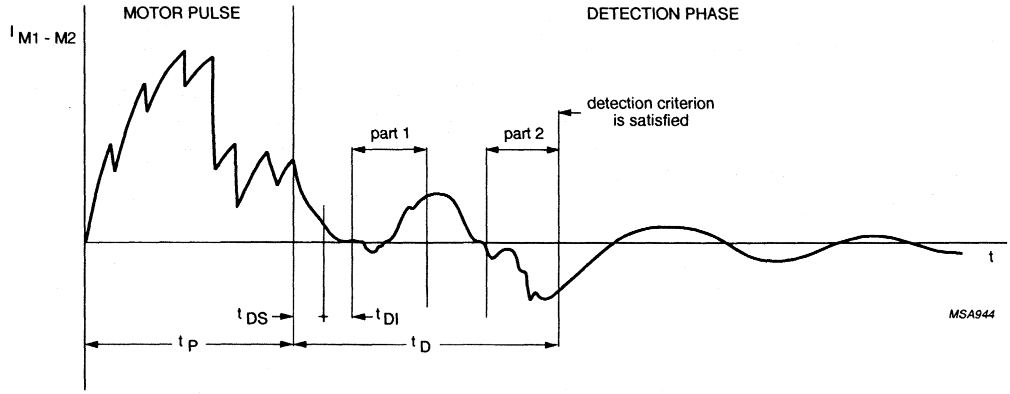


Fig.7 Typical current waveform of a successfully executed motor pulse.

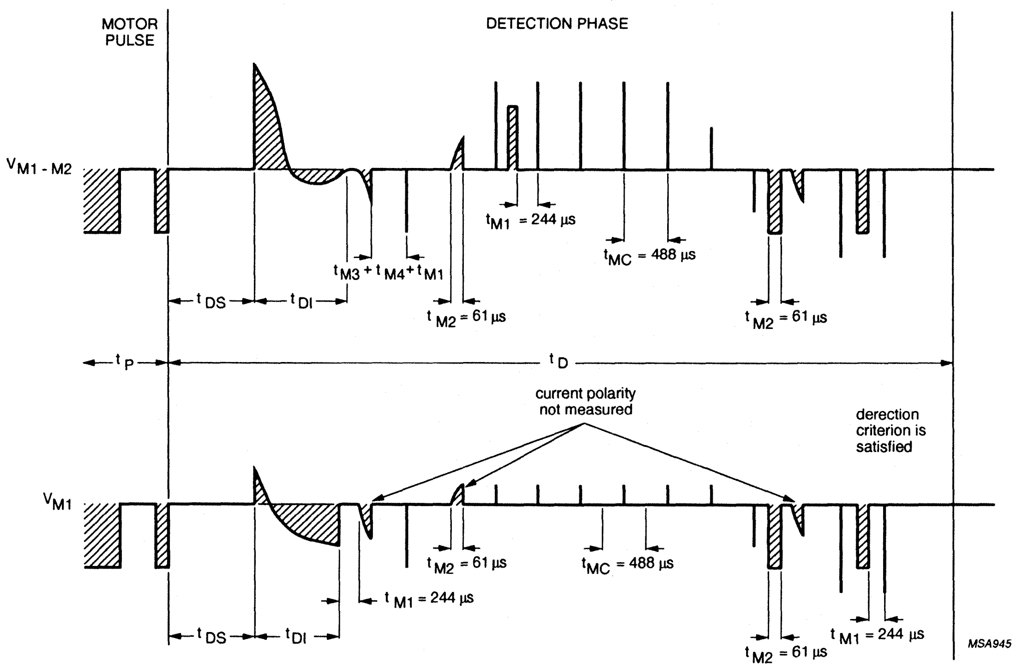


Fig.8 Detection phase of the current waveform in Fig.7.

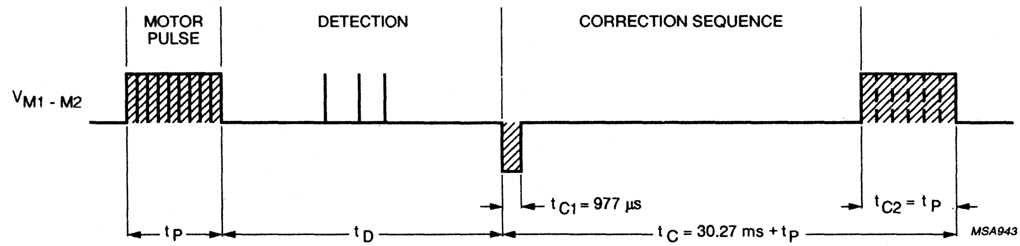


Fig.9 Correction sequence after a missing motor step with motor connected.

Time keeping adjustment

(1)

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 8192 Hz pulses are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig.11):

1. The quartz frequency deviation (Δf/f) and n are found (see Table 1).
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3}.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to write the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage between two motor pulses to return to operating mode.

(1). Programming can be performed 100 times.

Table 1 Quartz crystal frequency deviation and n.

$\frac{\Delta f}{f} \times 10^{-6}$ (ppm)	n	t_{T3} step 2 or 9 (ms)
0	0	31.250 (note 1)
+2.03	1	31.372
+4.06	2	31.494
.	.	.
.	.	.
.	.	.
+127.89	63	38.936

Note

1. 122 μs per step.

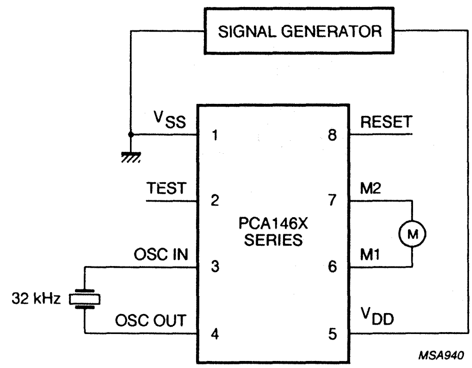
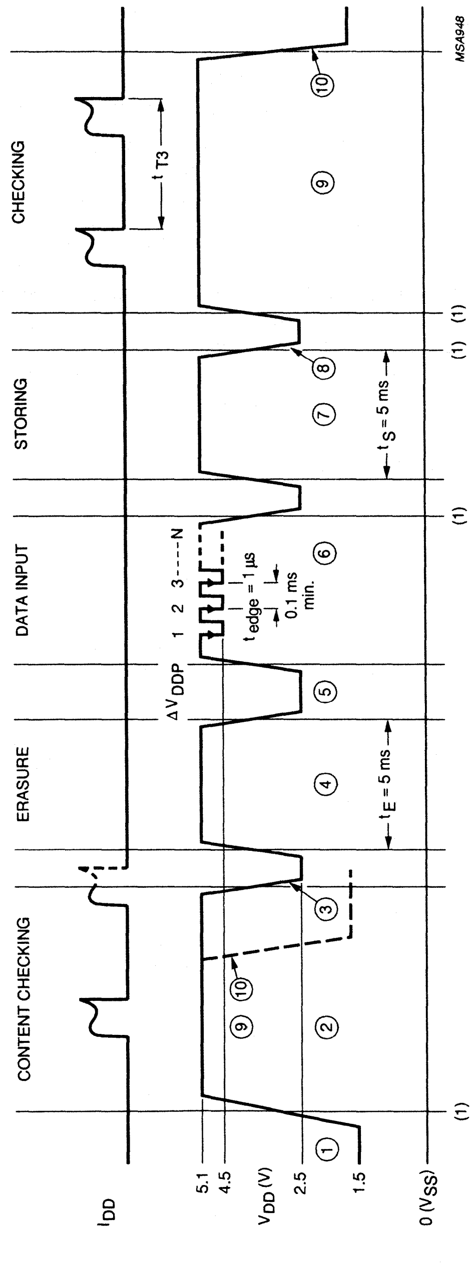


Fig.10 Programming circuit diagram.



(1) Rise and fall time should be greater than 400 µs/V for immediately correct checking.

Fig.11 V_{DD} for programming.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms. All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of the inhibition, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a 3-state mode and sets the motor pulse width for the next available motor pulse to stage 1 in the silver-oxide mode. A 32 Hz signal without jitter is produced at the TEST pin. Debounce time RESET = 14.7 to 123.2 ms.

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the inhibition.

Test 1 ($V_{DD} > V_{EOL}$): normal function takes place except the motor pulse period is t_{T1} = 125 ms instead of t_T and the motor pulse stage is reduced every second instead of every 8 minutes. At TEST a speeded-up 8 minute signal is available.

Test 2: if V_{DD} becomes lower than V_{EOL} motor pulses of stage 8 with a time period of t_{T2} = 31.25 ms are produced.

Test and reset mode are terminated by disconnecting the RESET pin.

Test 3: when V_{DD} voltage level is greater than 5.1 V, motor pulses of stage 8 with a time period of t_{T3} = 31.25 ms and n x 122 μs are produced to check the contents of the EEPROM. At TEST a speeded-up cycle for motor pulse period signal t_T is available at 1024 times its normal frequency. Decreasing V_{DD} voltage level to lower than 2.5 V between two motor pulses returns the circuit to normal operating conditions.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages	note 2	V_{SS}	V_{DD}	V
	output short-circuit duration			indefinite	
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD1}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.55	2.5	V
ΔV_{DD}	supply voltage	transient within 1.2 V and 2.5 V	–	–	0.25	V
V_{DD2}	supply voltage	programming	5.0	5.1	5.2	V
ΔV_{DDP}	supply voltage pulse	programming	0.55	0.6	0.65	V
I_{DD1}	supply current	between motor pulses	–	170	260	nA
I_{DD2}	supply current	V_{DD} = 2.1 V	–	190	300	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	–	180	280	nA
I_{DD4}	supply current	V_{DD} = 2.1 V	–	220	360	nA
I_{DD5}	supply current	T_{amb} = −10 to +60 °C	–	–	600	nA
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
R_{os}	output short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	–	200	300	mV
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)} \leq 50$ mV	6	15	–	µS
t_{osc}	start-up time		–	1	–	s
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		8	10	12	pF
C_o	output capacitance		12	15	18	pF
Voltage level detector						
V_{LIT}	threshold voltage		1.62	1.80	1.98	V
V_{EOL}	threshold voltage		1.30	1.38	1.46	V
ΔV_{EOL}	hysteresis of threshold		–	10	–	mV
$\frac{\Delta V_{EOL}}{dT}$	temperature coefficient		–	−1	–	mV/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	µs
I_{im}	peak input current	note 1	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA

Note

1. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 2 Available types.

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS					
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS
1461	U	1	7.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium
1462	U	1	5.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium
1463	U	1	3.9	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium
1464	U/10	0.5	3.9	81	P = 1 N = 2	no	no	no oscillator 3.0 V Lithium
1465	U/10; U/7	1	5.8	max. 100	P = 1 N = 2	yes	no	1.5 V
1466	T	5	5.8	max. 100 81	P = 1 N = 2	no	no	1.5 V and 2.1 V Lithium
1467	U/10	1	7.8	100	P = 1 N = 2	yes	no	

Where:

U = Chip in trays.

U/7 = Chip with bumps on tape.

U/10 = Chip on foil.

T = SOT144.

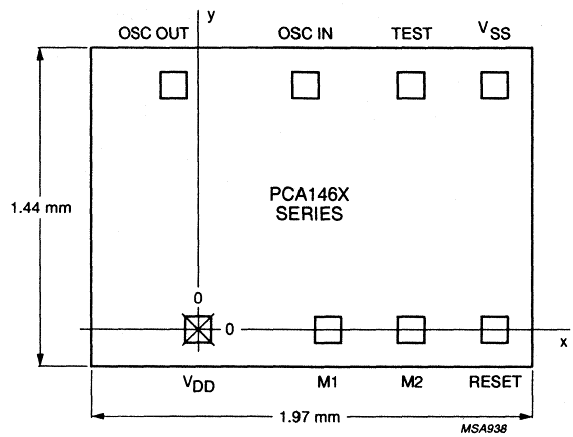
TIMING PARAMETERS

SYMBOL	PARAMETER	SECTION	VALUE	OPTION	UNIT
t_T	cycle for motor pulse (note 1)	motor pulse (Figs 3, 4 and 5)	1	5, 10, 12 or 20	s
t_P	motor pulse width		7.81	3.9 or 5.9	ms
t_{DF}	duty factor		977	–	µs
t_{ONL}	last duty factor on		61 to 305	–	µs
t_v	voltage detection cycle	level mode	60	–	s
t_{SON}	duty factor on	silver-oxide mode (Fig.4)	550 to 794	–	µs
t_{SOFF}	duty factor off		427 to 183	–	µs
t_{SONF}	first duty factor on		488	–	µs
t_{AOFF}	additional duty factor off	lithium mode (Fig.5)	183	–	µs
t_{LON}	duty factor on		305 to 611	–	µs
t_{LOFF}	duty factor off		672 to 366	–	µs
t_{LONF}	first duty factor on		244	–	µs
t_E	EOL sequence	end-of-life mode	4	–	s
t_{E1}	motor pulse width		t_P	–	ms
t_{E2}	time between pulses		31.25	–	ms
t_D	detection sequence	detection (Fig.8)	4.3 to 28.3	–	ms
t_{DS}	short-circuited motor		977	–	µs
t_{DI}	dissipation of energy		977	–	µs
t_{MC}	measurement cycle		488	–	µs
t_{M1}	phase 1		244	–	µs
t_{M2}	phase 2 (measure window)		61	–	µs
t_{M3}	phase 3		122	–	µs
t_{M4}	phase 4		61	–	µs
P	positive current polarities		1	$P < N$	
N	negative current polarities		2	2 to 6	
t_C	correction sequence	correction sequence (Fig.9)	$t_P + 30.27$	–	ms
t_{C1}	small pulse width		977	–	µs
t_{C2}	large pulse width		t_P	–	ms
	cycles for motor-pulses in:	testing			
t_{T1}	test 1		125	–	ms
t_{T2}	test 2		31.25	–	ms
t_{T3}	test 3	Fig.11	31.25 to 39	–	ms
t_{DEB}	debounce time for RESET = V_{DD}		14.7 to 123.2	–	ms

Note

1. No option available when EOL indication is required.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 2.84 mm².

Bonding pad dimensions: 110 µm x 110 µm.

Chip thickness: 200 ±25 µm, with bumps: 270 ±25 µm.

Fig.12 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in µm).
All x/y coordinates are referenced to bottom left pad (V_{DD}), see Fig.12.

PAD	X	Y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−495	−170

32 kHz watch circuit with adaptive motor pulse

PCA148X series

FEATURES

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- High immunity of the oscillator to leakage currents
- Time keeping adjustment electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption; typically 170 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current compared with conventional circuits, by self adaption of the motor pulse width in accordance with the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

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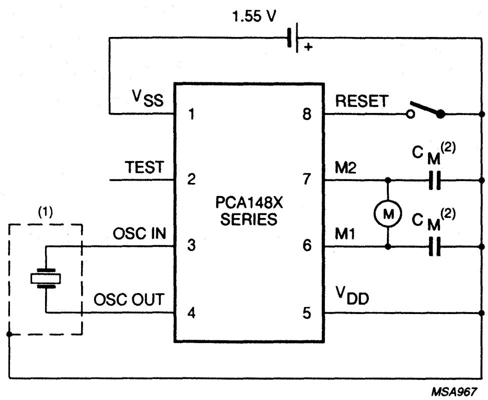
PCA148XT	8	micro-flat-pack	plastic	SOT144A
PCA148XU	–	chip in tray	–	–



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} or V_{SS} should be less than C_M = 80 pF for correct operation of the detection circuit. Driving the motor at its minimum energy, probe and stray capacitance must be avoided.

Fig.1 Typical application circuit diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

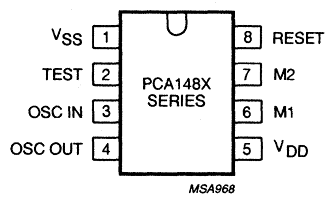


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different stages depending on the torque required to turn the motor (Fig.4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. When a step is missed a correction sequence will be started (Fig.3).

Motor pulses

The circuit produces motor pulses of six different stages (stage 1 to 5, stage 6).

Stages 1 to 5 are used in normal operation, stage 6 occurs under the following conditions:

- correction pulse after a missing step
- end-of-life mode
- if stage 5 is not enough to turn the motor.

The ON state of the motor pulse varies between 43.75% and 75% of the duty factor t_{DF} = 977 μs depending on the stage (Fig.4). It increases in steps of 6.25% per stage.

After a RESET the circuit always starts and continues with stage 1, when all motor pulses have been executed. A failure to execute all motor pulses results in the circuit going into stage 2, this sequence will be repeated through to stage 6.

When the motor pulses at stage 5 are not large enough to turn the motor, stage 6 is implemented for a maximum of 8 minutes with no attempt to keep current consumption low. After stage 6 has been executed the procedure is repeated from RESET.

The circuit operates for 8 minutes at a fixed stage, if every motor pulse is executed. The next 480 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and for a maximum of 8 minutes the motor pulses are increased by one stage.

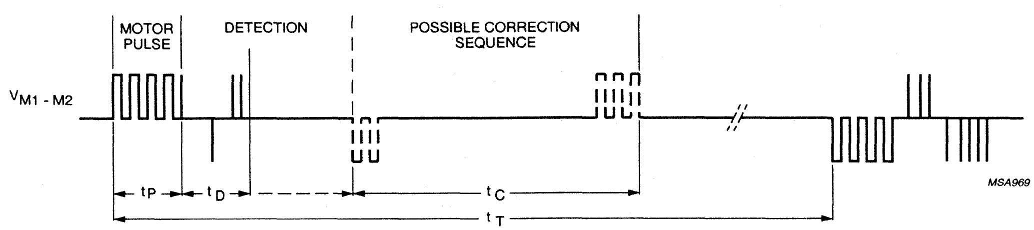
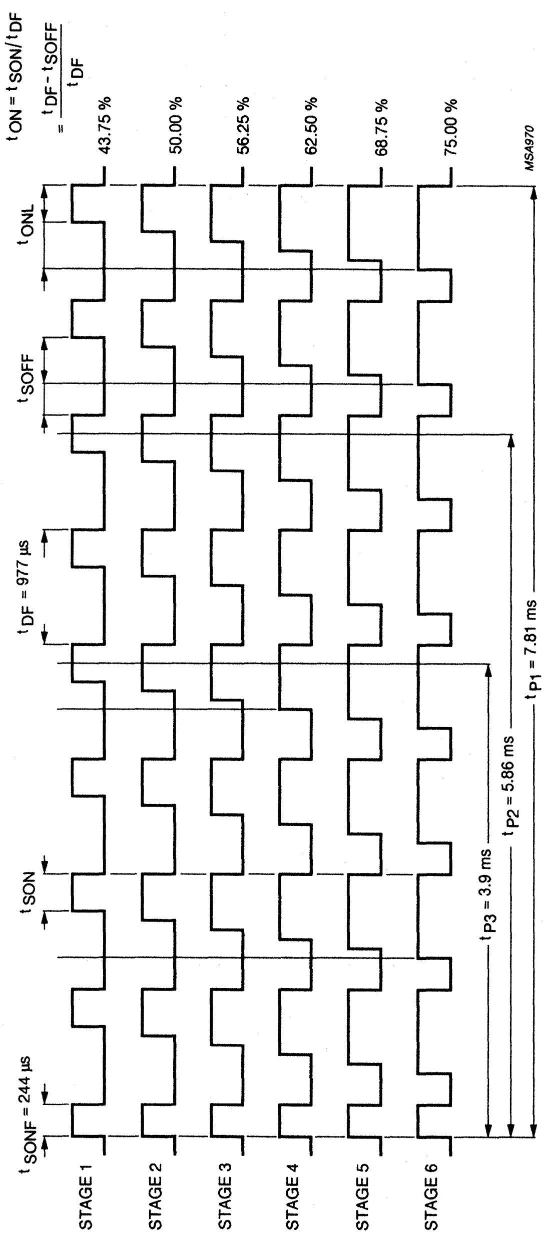


Fig.3 Possible motor output waveform in normal operation with motor connected.



t_{OFF} for stage 1 to 6 = 611 µs – stage x 61 µs

t_{ON} for stage 1 to 6 = 366 µs + stae x 61 µs

Fig.4 Motor pulses (V_{DD} = 1.55 V).

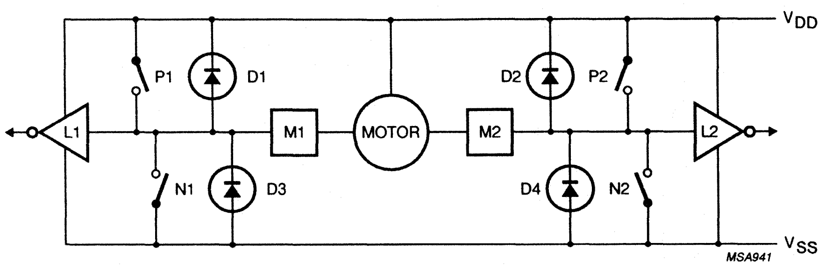


Fig.5 Motor driving and detecting circuit.

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{EOL} every minute. The first voltage level detection is carried out 30 ms after RESET.

When the detected V_{DD} voltage level is greater than V_{EOL}, the circuit operates in normal mode (Fig.4).

If the battery end-of-life is detected ($V_{DD} < V_{EOL}$), the detection and stage control is switched OFF and the waveform of stage 6 will be executed. To indicate this condition the waveform is produced in bursts of 4 pulses every 4 s.

Detection of motor movement

After a motor pulse, the motor is short-circuited to V_{DD} for 1 ms. Afterwards the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig.5 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1. Then the first of 52 possible measurement cycles (t_{MC}) starts to measure the induced current.

Detection criterion (Figs 6 and 7)

Part 1

- P = 2 number of measured positive current polarities after t_{DI}.

Part 2

- N = 3 number of measured positive current polarities since the first negative current polarity is detected after part 1 (see Fig.6).

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

Every measurement cycle (t_{MC}) has 4 phases. They are as follows:

SYMBOL	PHASE	DESCRIPTION
t_{M1}	1	During T_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.
t_{M2}	2	Measures the induced current; during a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is short-circuited to V_{DD}. Depending on the direction of the interrupted current: - the current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2; - the current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1. A succesfully detected current polarity is normally characterized by a short pulse of 0.5 to 10 μs with a voltage up to ±2.1 V, failed polarity detection by the maximum pulse width of 61 μs and a voltage of ±0.5 V (see Fig.7).
t_{M3}	3	The switches P1 and P2 remain closed for the time t_{M3}.
t_{M4}	4	If the circuit detects less pulses than P and N respectively, a pulse of the time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed. Otherwise P1 and P2 remain closed.

Detection and pulse width control will be switched OFF, when the battery voltage is below the end-of-life voltage (V_{EOL}) or if stage 5 is not sufficient to turn the motor.

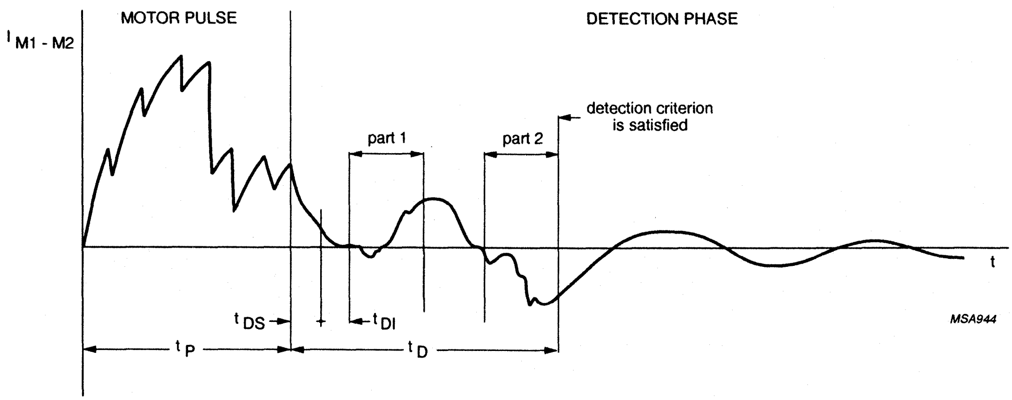


Fig.6 Typical current waveform of a successfully executed motor pulse.

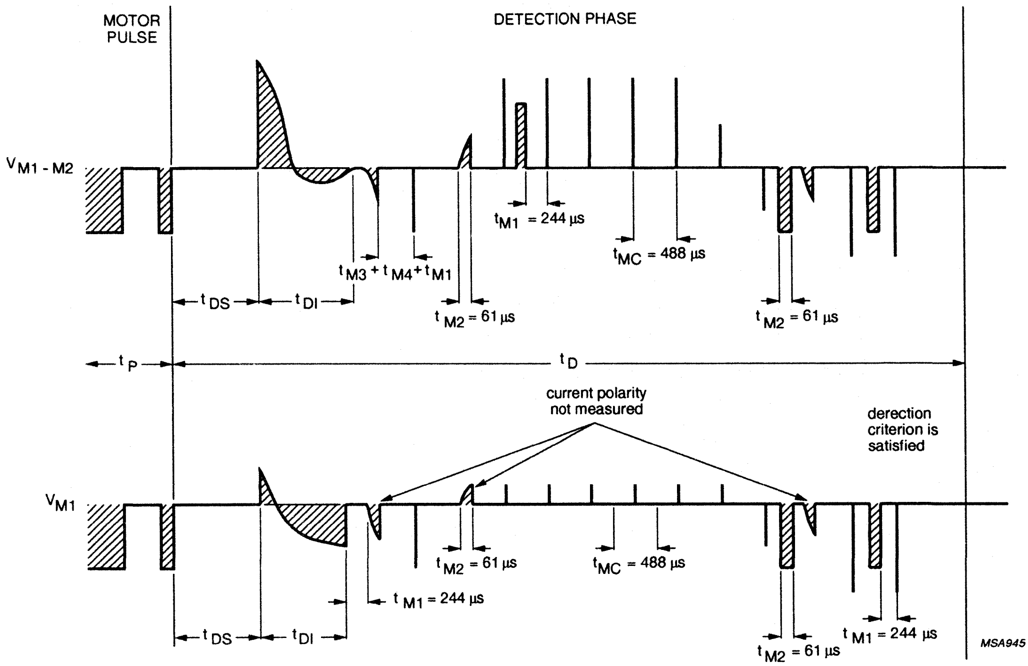


Fig.7 Detection phase of the current waveform in Fig.6.

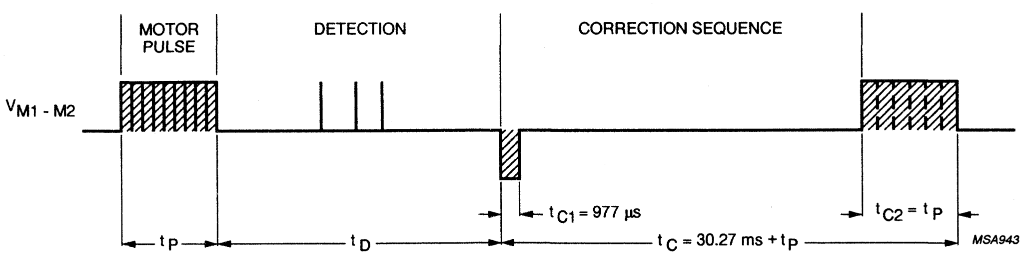


Fig.8 Correction sequence after a missing motor step with motor connected.

Correction sequence

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 29.30 ms a pulse of stage 6 (t_{C2}) to turn the motor.

Time keeping adjustment

(1)

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 8192 Hz pulses are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig.10):

1. The quartz frequency deviation ($\Delta f/f$) and n are found (see Table 1).
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3}.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to write the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage between two motor pulses to return to operating mode.

Table 1 Quartz crystal frequency deviation and n.

$\frac{\Delta f}{f} \times 10^{-6}$ (ppm)	n	t_{T3} step 2 or 9 (ms)
0	0	31.250 (note 1)
+2.03	1	31.372
+4.06	2	31.494
.	.	.
.	.	.
.	.	.
+127.89	63	38.936

Note

1. 122 µs per step.

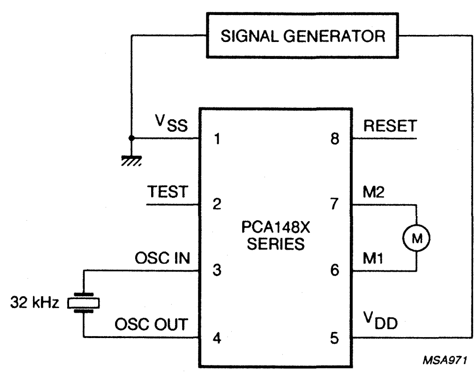
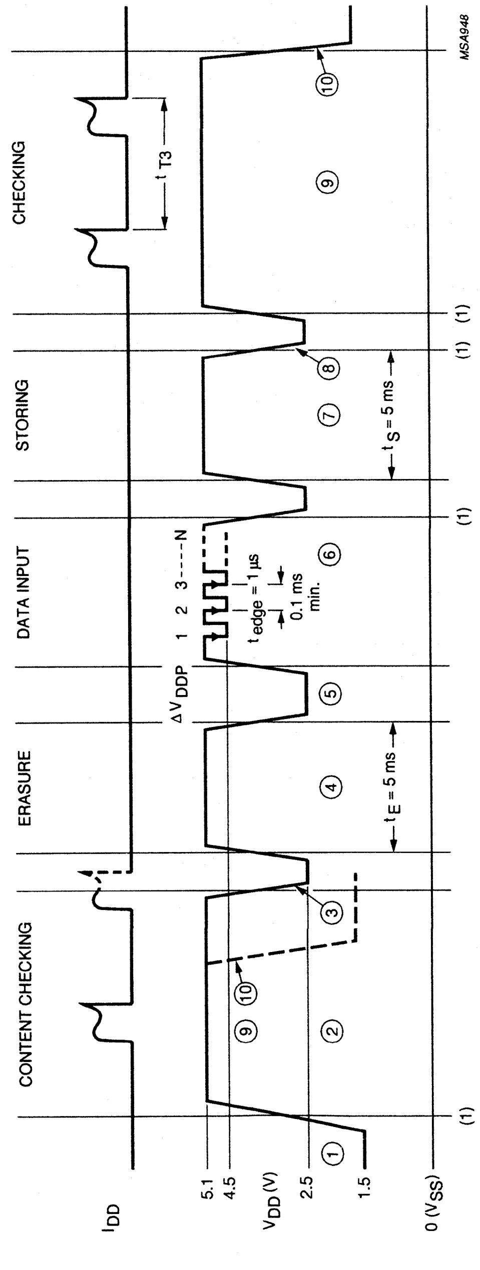


Fig.9 Programming circuit diagram.

(1) Programming can be performed 100 times.



(1) Rise and fall time should be greater than 400 µs/V for immediately correct checking.

Fig.10 V_{DD} for programming.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms. All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of the inhibition, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a 3-state mode and sets the motor pulse width for the next available motor pulse to stage 1. A 32 Hz signal without jitter is produced at the TEST pin. Debounce time RESET = 14.7 to 123.1 ms.

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the inhibition.

Test 1 ($V_{DD} > V_{EOL}$): normal function takes place except the motor pulse period is t_{T1} = 125 ms instead of t_T and the motor pulse stage is reduced every second instead of every 8 minutes. At TEST a speeded-up 8 minute signal is available.

Test 2: if V_{DD} becomes lower than V_{EOL} motor pulses of stage 6 with a time period of t_{T2} = 31.25 ms are produced.

Test and reset mode are terminated by disconnecting the RESET pin.

Test 3: when V_{DD} voltage level is greater than 5.1 V, motor pulses without chopping and a time period of t_{T3} = 31.25 ms and n x 122 µs are produced to check the contents of the EEPROM. At TEST a speeded-up cycle for motor pulse period signal t_T is available at 1024 times its normal frequency. Decreasing V_{DD} voltage level to lower than 2.5 V between two motor pulses returns the circuit to normal operating conditions.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages	note 2	V_{SS}	V_{DD}	V
	output short-circuit duration		indefinite		
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD1}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.55	2.5	V
ΔV_{DD}	supply voltage	transient	–	–	0.25	V
V_{DD2}	supply voltage	programming	5.0	5.1	5.2	V
ΔV_{DDP}	supply voltage pulse	programming	0.55	0.6	0.65	V
I_{DD1}	supply current	between motor pulses	–	170	260	nA
I_{DD2}	supply current	T_{amb} = −10 to +60 °C	–	–	600	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	–	180	280	nA
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
R_{os}	output short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	–	200	300	mV
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)} \leq 50$ mV	6	15	–	µS
t_{osc}	start-up time		–	1	–	s
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		8	10 (note 1)	12	pF
C_o	output capacitance		12	15 (note 1)	18	pF
Voltage level detector						
V_{EOL}	threshold voltage		1.30	1.38	1.46	V
ΔV_{EOL}	hysteresis of threshold		–	10	–	mV
$\frac{\Delta V_{EOL}}{dT}$	temperature coefficient		–	−1	–	mV/K
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	µs
I_{im}	peak input current	note 2	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA

Notes

1. PCA1484: C_i typ. 8 pF; C_o typ. 12 pF.
2. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 2 Available types.

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS					
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS
1482	U; U/7; T	1	5.8	75	P = 2 N = 3	yes	yes	
1483	U/7	1	5.8	75	P = 2 N = 3	yes	no	
1484	U/7	20	5.8	75	P = 2 N = 3	yes	no	C_i = 8 pF 2.1 V C_o = 12 pF
1485	U/7	1	5.8	75	P = 1 N = 2	yes	yes	
1486	U/7	1	5.8	75	P = 1 N = 2	yes	no	
1487	U/5; T	1	7.8	75	P = 2 N = 3	yes	yes	

Where:

U = Chip in trays.

U/5 = Wafer.

U/7 = Chip with bumps on tape.

T = SOT144.

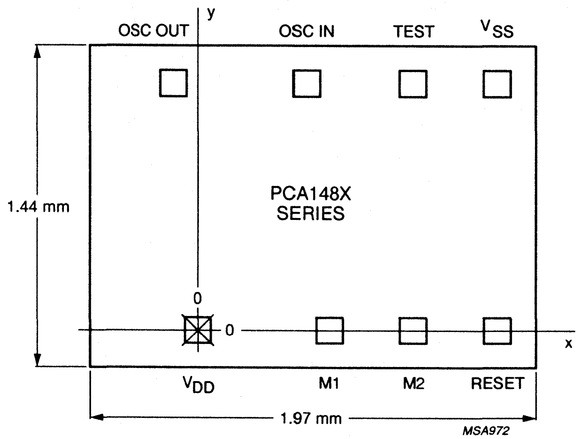
TIMING PARAMETERS

SYMBOL	PARAMETER	SECTION	VALUE	OPTION	UNIT
t_T	cycle for motor pulse (note 1)	motor pulse (Figs 3 and 4)	1	5, 10, 12 or 20	s
t_P	motor pulse width		7.81	3.9 or 5.9	ms
t_{DF}	duty factor		977	–	µs
t_{ONL}	last duty factor on		183 to 488	–	µs
t_v	voltage detection cycle	level mode	60	–	s
t_{SON}	duty factor on	silver-oxide mode (Fig.4)	427 to 733	–	µs
t_{SOFF}	duty factor off		550 to 244	–	µs
t_{SONF}	first duty factor on		244	–	µs
t_E	EOL sequence	end-of-life mode	4	–	s
t_{E1}	motor pulse width		t_P	–	ms
t_{E2}	time between pulses		31.25	–	ms
t_D	detection sequence	detection (Fig.7)	4.3 to 28.3	–	ms
t_{DS}	short-circuited motor		977	–	µs
t_{DI}	dissipation of energy		977	–	µs
t_{MC}	measurement cycle		488	–	µs
t_{M1}	phase 1		244	–	µs
t_{M2}	phase 2 (measure window)		61	–	µs
t_{M3}	phase 3		122	–	µs
t_{M4}	phase 4		61	–	µs
P	positive current polarities		2	$P < N$	
N	negative current polarities		3	2 to 6	
t_C	correction sequence	correction sequence (Fig.8)	$t_P + 30.27$	–	ms
t_{C1}	small pulse width		977	–	µs
t_{C2}	large pulse width		t_P	–	ms
	cycles for motor-pulses in:	testing			
t_{T1}	test 1		125	–	ms
t_{T2}	test 2		31.25	–	ms
t_{T3}	test 3	Fig.10	31.25 to 39	–	ms
t_{DEB}	debounce time for RESET = V_{DD}		14.7 to 123.1	–	ms

Note

1. No option available when EOL indication is required.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 2.84 mm².

Bonding pad dimensions: 110 μm x 110 μm.

Chip thickness: 200 ±25 μm, with bumps: 270 ±25 μm.

Fig.11 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to bottom left pad (V_{DD}), see Fig.11.

PAD	X	Y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−495	−170

32 kHz watch circuit with frequency adjustment

PCA159X series

FEATURES

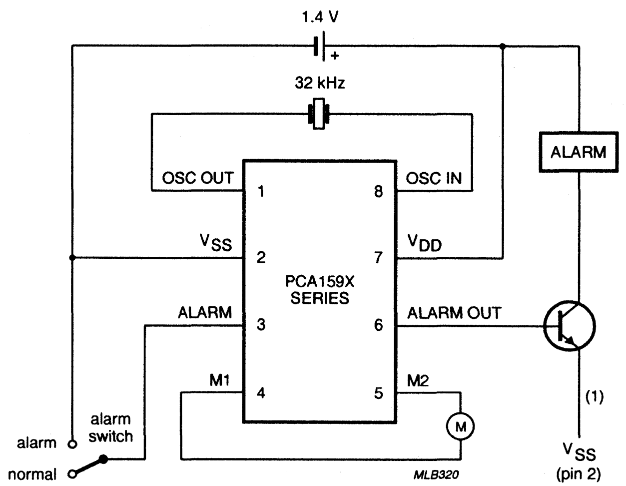
- 32 kHz oscillator frequency
- Low current consumption; typically 1.5 μA, maximum 5 μA
- Low minimum supply voltage: 1.1 V
- Alarm input
- Motor test
- Test mode speed-up for fast testing
- Quartz frequency electrically programmable and reprogrammable (via EEPROM)
- Protected against electrostatic charges.

GENERAL DESCRIPTION

The PCA159X series are silicon-gate CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled clocks, with a bipolar stepping motor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA159XP	8	DIL	plastic	SOT97
PCA159XT	8	mini-pack	plastic	SO8; SOT96C
PCA159XU/10	–	chip on film frame carrier (FFC)	–	–



(1) The emitter of the transistor must be connected to V_{SS}, except when used as a replacement for the PCA158X series where it must be connected to pin 3; in this event the base of the alarm transistor must be connected via a 1 kΩ series resistor.

Fig.1 Typical application circuit diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC OUT	1	oscillator output
V_{SS}	2	ground (0 V)
ALARM/TEST IN	3	alarm and test input
M1	4	motor 1 output
M2	5	motor 2 output
ALARM OUT	6	alarm output
V_{DD}	7	supply voltage
OSC IN	8	oscillator input

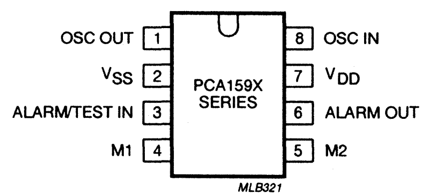


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Operating mode

The alarm input (pin 3) is left open-circuit. An output frequency of 256 Hz is provided at pin 3 for test purposes.

Alarm mode

The alarm input is connected to V_{SS}. The alarm signal in accordance with Fig.4 is provided at pin 6.

Test mode

The circuit must be in normal operating mode for at least 10 ms before entering test mode.
The test mode consists of two parts:

MOTOR TEST

The alarm input is connected to V_{DD}. In this test mode the motor output period is 125 ms (all types) and the motor pulse width is identical to that of the normal mode. The alarm output periods are also increased by a factor of 128. The alarm modulation is also suppressed.

IC TEST (IC SUPPLIER ONLY)

The customer uses this mode during frequency programming. On the negative edge of the first positive pulse (see Fig.8) the IC test is enabled. The motor output is increased by a factor of 1024. The duty factor in this mode is 1:1. The alarm mode is disabled.

On the positive edge of the second pulse (corresponding to the first program pulse) the motor test mode is re-selected.

To disable the test mode, pin 3 must be left open-circuit or connected to V_{SS}.

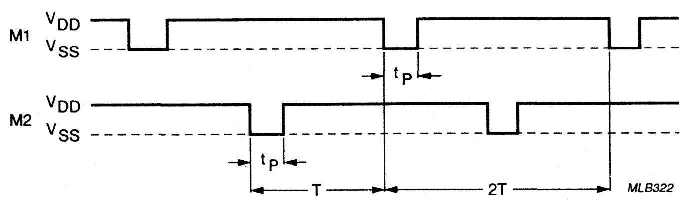


Fig.3 Motor output waveforms.

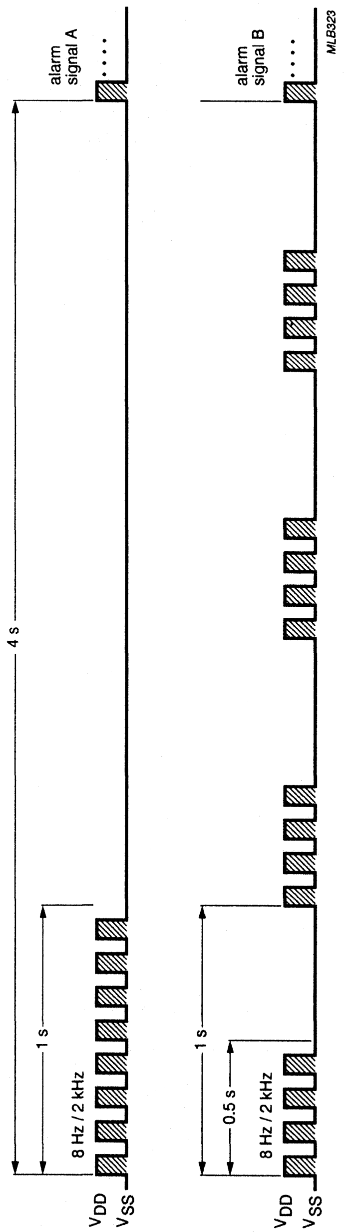


Fig.4 Alarm output waveforms.

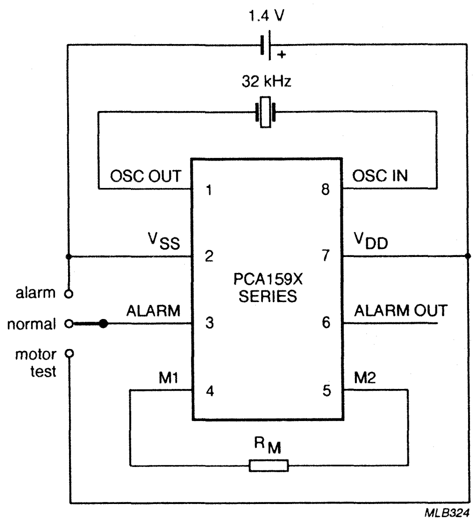


Fig.5 Test and test speed-up circuit.

Frequency trimming

Frequency trimming is carried out by electrically programming the oscillator input capacitance to one of 64 values contained within the non-volatile memory. This is accomplished by carrying out the following five steps; Figs 6, 7, 8 and 9 illustrate this procedure.

1. ERASING

With V_{SS} = −1.4 V, the generator (pin 3) is taken from −1.4 V to 0 V. The device is now in test mode. Erasure is carried out by increasing V_{SS} to −5.5 V and setting the generator (pin 3) to +1.4 V.

2. CHECKING ERASING/ZERO

With V_{SS} = −1.4 V, the generator (pin 3) is taken from −1.4 V to 0 V. The device is in test mode and minimum capacitance is obtained.

3. MEASURE/DATA INPUT

On the first 1.4 V pulse (pin 3) the test mode is changed from motor test to IC test. This pulse releases the program register thus allowing the frequency to be programmed. The positive edge of the second pulse switches the IC test mode back to the motor test mode. The negative edge of the second pulse increases the capacitance by one unit, this occurs on all the subsequent pulses. The frequency can be measured between these increases. This procedure is repeated until the required frequency is obtained. If the adjustment to the frequency is greater than required, the procedure can be restarted with step 2.

4. WRITING

The capacitance is fixed by increasing V_{SS} to −5.5 V.

5. CHECKING WRITING

With V_{SS} = −1.4 V, the generator (pin 3) is taken from −1.4 V to 0 V. The device is in test mode and trimmed capacitance is obtained. The frequency can be checked.

Note

The information concerning the capacitive value is obtained from the EEPROM cells and the program register. Therefore the program register must be reset before the frequency can be measured (see steps 1 to 5). Programming can be performed 100 times.

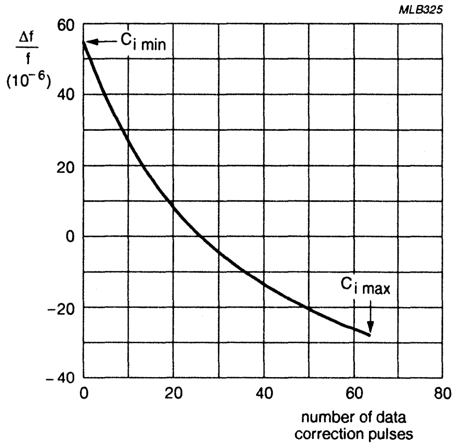
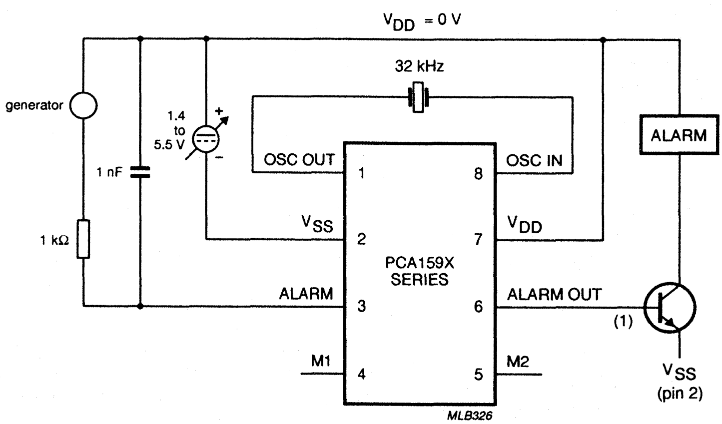


Fig.6 Typical frequency characteristic; C_1 = 2.8 fF, C_0 = 3 pF, C_L = 10 pF, f = 32.768 kHz.



(1) During programming ALARM OUT is active LOW, so that programming is possible when the alarm transistor is connected to pin 6.

Fig.7 Frequency trimming circuit.

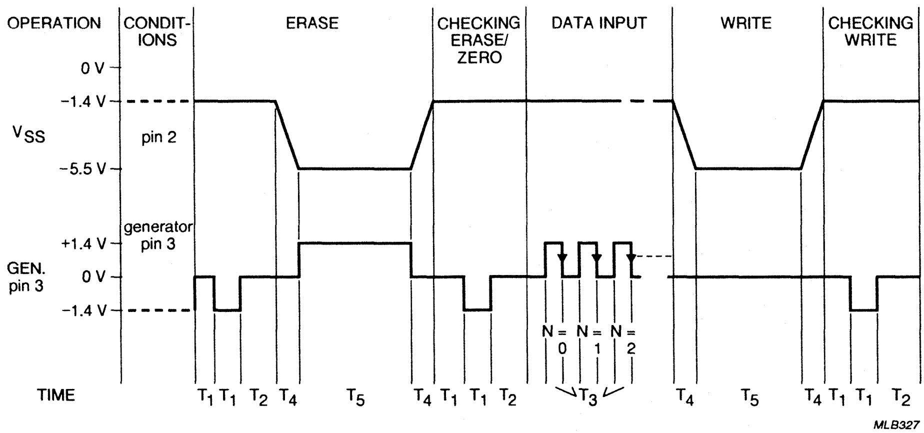


Fig.8 Frequency trimming signals (V_{DD} = 0 V).

Table 1 Frequency trimming timing requirements.

TIME	SYMBOL	MIN.	MAX.	UNIT
Reset time 1	T_1	1	–	ms
Reset time 2	T_2	5	–	ms
Data pulse width/gap	T_3	100	–	µs
Supply rise/fall time	T_4	1	–	ms
WRITE/ERASE time	T_5	10	–	ms

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SS}	supply voltage	V_{DD} = 0 V; note 1	+1.8	−6	V
V_I	all input voltages except pin 3	note 2	V_{SS}	V_{DD}	V
V_{3-2}	input voltage at pin 3		V_{SS}	V_{DD}+1	V
	output short-circuit duration at pins 4, 5 and 6			indefinite	
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+125	°C
R_{ESD}	resistance against electrostatic discharge			note 3	

Notes

1. Connecting the battery at 1.8 V maximum with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Three discharges of a 100 pF capacitor at 800 V, via a 1.5 kΩ resistor (with positive and negative polarity).

CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −1.4 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 10 pF; C_0 = 3 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS1}	supply voltage	operating	−1.1	–	−1.8	V
V_{SS2}	supply voltage	starting	−1.2	–	–	V
V_{SS3}	supply voltage	programming	−5.4	−5.5	−5.6	V
I_{DD}	supply current	$R_L = \infty$	–	1.5	5.0	µA
Motor output (pins 4 and 5)						
t_T	period	note 1	1.0	–	60.0	s
t_P	pulse width	note 1	3.9	–	62.5	ms
I_M	current into load	R_M = 200 Ω; V_{SS} = −1.2 V	4.3	–	–	mA
R_O	output impedance	R_M = 200 Ω	–	50	–	Ω
Alarm output (pin 6)						
	output waveforms	see Fig.4				
I_{sink}	sink current	R = 10 Ω; V_{SS} = −5.5 V	–	200	–	µA
I_{source}	source current	R = 1 Ω; V_{SS} = −1.2 V	0.3	1.0	–	mA
Alarm test input (pin 3)						
t_d	input delay time		–	–	70	ms
I_I	input current	note 2 V_{SS} = −5.5 V	 – –	 2 50	 – –	 µA µA
Oscillator (pins 1 and 8)						
R_p	polarization resistance		3	10	30	MΩ
C_O	output capacitance (pin 1)		–	24	–	pF
C_I	input capacitance data pulses (pin 8)	n = 0; note 3	–	9	–	pF
ΔC_I	input capacitance steps		–	0.25	–	pF
$\Delta f/f$	frequency stability	ΔV_{SS} = 100 mV; n = 20	–	0.6 x 10^{-6}	–	
t_{ret}	data retention time	T_{amb} = −10 to +60 °C	–	10	–	years

Notes

1. See Table 2 for the typical values.
2. These are average values for the 256 Hz output with 1:1 duty factor.
3. Number of data correction pulses (n).

Table 2 Available types.

TYPE NUMBER	DELIVERY FORMAT	MOTOR OUTPUT				ALARM SIGNAL (see Fig.4)
		PERIOD t_T (s)	PULSE WIDTH t_P (ms)	MINIMUM CURRENT I_M (mA)	EEPROM	
1593		1	31.25	4.3	yes	B
1594		1	46.8	4.3	yes	A
1595		1	46.8	4.3	yes	B
1596		1	15.6	4.3	yes	A
1597		4	15.6	4.3	yes	B

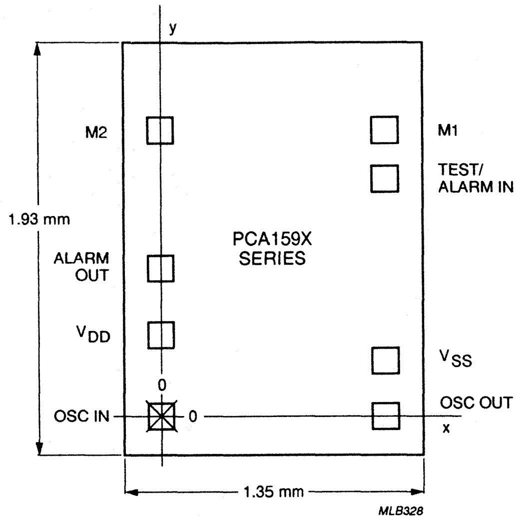
Where:

P = SOT97.

T = SOT96C.

U/10 = Chip on film frame carrier (FFC).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 2.61 mm².

Bonding pad dimensions: 110 μm x 110 μm.

Fig.9 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to bottom left pad (OSC IN), see Fig.9.

PAD	X	Y
OSC OUT	1006	0
V_{SS}	1006	220
TEST/ALARM IN	1006	1111
M1	1006	1296
M2	0	1296
ALARM OUT	0	651
V_{DD}	0	376
OSC IN	0	0
chip corner (max. value)	−202	−225

FEATURES

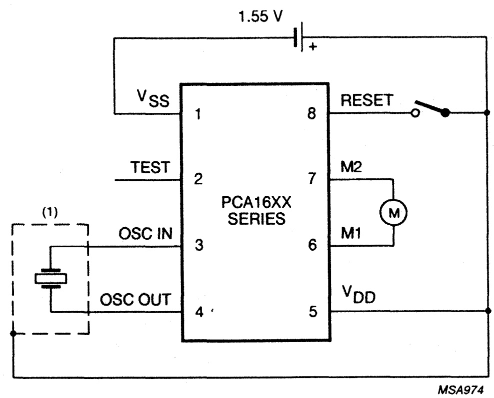
- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Time keeping adjustment electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption; typically 170 nA
- Detector for silver-oxide or lithium battery voltage levels
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA16XX series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA16XXT	8	micro-flat-pack	plastic	SOT144A
PCA16XXU	–	chip in tray	–	–



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

Fig.1 Typical application circuit diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	positive supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

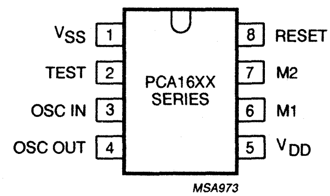


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Motor pulse

The motor pulse width (t_W) and the cycle times (t_T) are given in Table 2.

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{LIT} and V_{EOL} every minute. The first voltage level detection is carried out 30 ms after a RESET.

Lithium mode

If a lithium voltage is detected ($V_{DD} \geq V_{LIT}$), the circuit will operate in the lithium mode. The motor pulse will be produced with a 75% duty factor.

Silver-oxide mode

If the voltage level detected is between V_{LIT} and V_{EOL}, the circuit will operate in silver-oxide mode.

Battery end-of-life

(1)

If the battery end-of-life is detected ($V_{DD} \leq V_{EOL}$), the motor pulse will be produced without chopping. To indicate this condition, bursts of 4 pulses are produced every 4 s.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms. All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of time keeping adjustment, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a HIGH impedance 3-state condition and a 32 Hz signal without jitter is produced at the TEST pin. A debounce circuit protects accidental stoppages due to mechanical shock to the watch (t_{DEB} = 14.7 to 123.2 ms).

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the time keeping adjustment.

Test 1 ($V_{DD} > V_{EOL}$): normal function takes place except the voltage detection cycle (t_V) is 125 ms and the cycle time is 31.25 ms. At pin TEST a minute signal is available at 8192 times its normal frequency.

Test 2[(2)] ($V_{DD} < V_{EOL}$): the voltage detection cycle (t_V) is 31.25 ms and the motor pulse period (t_{T2}) = 31.25 ms.

Test and reset mode are terminated by disconnecting the RESET pin.

(1) Only available for types with a 1 s motor pulse.
(2) Only applicable for types with the battery end-of-life detector.

Test 3: when V_{DD} voltage level is greater than 5 V, motor pulses with a time period of t_{T3} = 31.25 ms and n x 122 µs are produced to check the contents of the EEPROM. At pin TEST the motor pulse period signal (t_T) is available at 1024 times its normal frequency. The circuit returns to normal operation when V_{DD} < 2.5 V between two motor pulses.

Time keeping adjustment

(1)

To compensate for the tolerance in the quartz crystal frequency, a number (n) of 8192 Hz pulses are inhibited every minute of operation. The number (n) is stored in a non-volatile memory, which is achieved by the following steps (see Fig.4):

1. The quartz frequency deviation (Δf/f) and n are found (see Table 1).
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3}.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to write the EEPROM and reset the circuit.
8. V_{DD} is decreased to the operating voltage level to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage between two motor pulses to return to operating mode.

Table 1 Quartz crystal frequency deviation and n.

$\frac{\Delta f}{f} \times 10^{-6}$ **(ppm)**	**n**	t_{T3} **step 2 or 9 (ms)**
0	0	31.250 (note 1)
+2.03	1	31.372
+4.06	2	31.494
.	.	.
.	.	.
.	.	.
+127.89	63	38.936

Note

1. 122 µs per step.

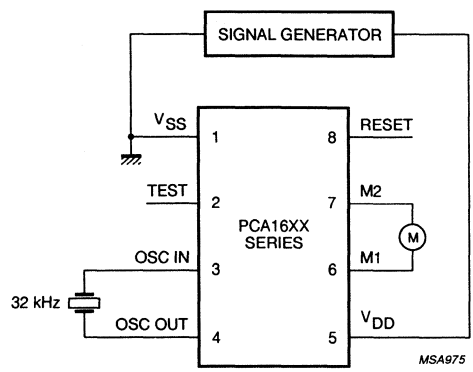
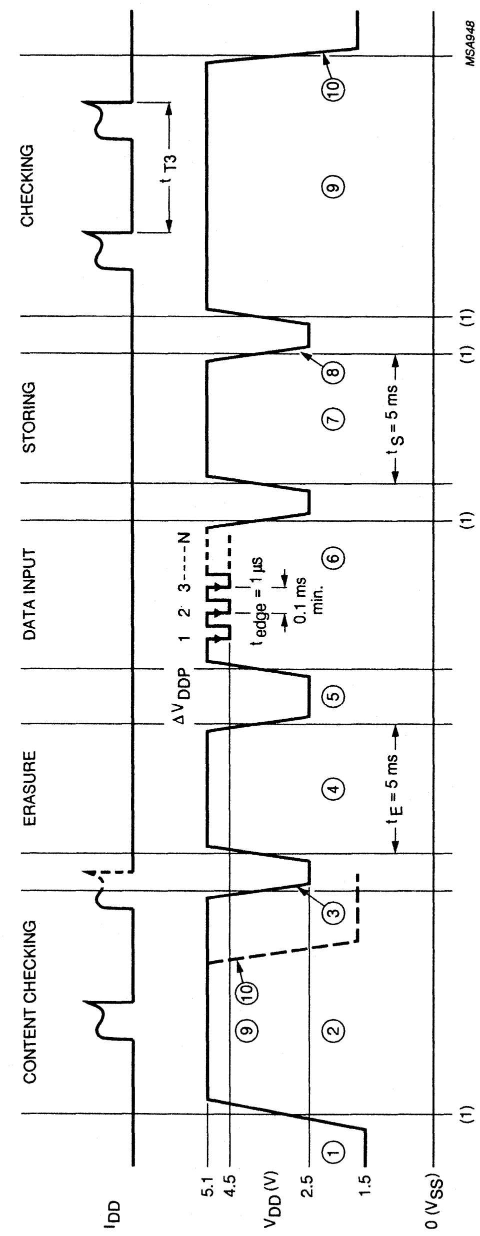


Fig.3 Programming circuit diagram.

(1) Programming can be performed 100 times.



(1) Rise and fall time should be greater than 1 ms for immediately correct checking.

Fig.4 V_{DD} for programming.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages	note 2	V_{SS}	V_{DD}	V
	output short-circuit duration		indefinite		
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C
V_{es}	electrostatic handling	note 3	−800	+800	V

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Equivalent to three discharges of a 100 pF capacitor at 800 V, through a resistor of 1.5 kΩ (with positive and negative polarity).

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.
Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.5	2.5	V
ΔV_{DD}	supply voltage	transient; V_{DD} = 1.2 to 2.5 V	–	–	0.25	V
V_{DDP}	supply voltage	programming	5.0	5.1	5.2	V
ΔV_{DDP}	supply voltage pulse	programming	0.55	0.6	0.65	V
I_{DD1}	supply current	between motor pulses	–	170	260	nA
I_{DD2}	supply current	between motor pulses; V_{DD} = 2.1 V	–	190	300	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	–	180	280	nA
I_{DD4}	supply current	stop mode; pin 8 connected to V_{DD}; V_{DD} = 2.1 V	–	220	360	nA
I_{DD5}	supply current	V_{DD} = 2.1 V; T_{amb} = −10 to +60 °C	–	–	600	nA
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_L = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
R_{sc}	short-circuit resistance Σ (P + N)	$I_{transistor}$ < 1 mA	–	200	300	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_T	cycle time		note 1			
t_P	pulse width		note 2			
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)} \leq 50$ mV	6	15	–	μA/V
t_{osc}	start-up time		–	1	–	s
Δf/f	frequency stability	$\Delta V_{DD} = 100$ mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		8	10	12	pF
C_o	output capacitance		12	15	18	pF
Voltage level detector						
V_{LIT}	threshold voltage	lithium mode	1.65	1.80	1.95	V
V_{EOL}	threshold voltage	battery end-of-life	1.27	1.38	1.46	V
ΔV_{VLD}	hysteresis of threshold		–	10	–	mV
$\frac{\Delta V_{VLD}}{°C}$	temperature coefficient		–	–1	–	mV/K
t_V	voltage detection cycle		–	60	–	s
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	μs
I_{im}	peak input current	note 3	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA
Test mode						
	cycle time:					
t_{T1}	test 1		–	31.25	–	ms
t_{T2}	test 2		–	31.25	–	ms
t_{T3}	test 3		see Table 1			
t_{DEB}	debounce time	RESET = V_{DD}	14.7	–	123.2	ms
Battery end-of-life						
t_{EOL}	end-of-life sequence		–	4	–	s
t_{E1}	motor pulse width	see Table 2	–	t_P	–	ms
t_{E2}	time between pulses		–	31.25	–	ms

Notes

1. Cycle time can be changed to one of the following values: 1, 5, 10, 12 or 20 s (see Table 2).
2. Pulse width can be varied from 2 ms to 15.7 ms in steps of 1 ms (see Table 2).
3. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 2 Available types and timing information (see Fig.5).

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS				
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS
1602	T	1	7.8	75	yes	no	
1603	U/7	20	7.8	100	yes	no	
1604	U; T	5	7.8	75	yes	no	
1605	U/7	5	4.8	75	yes	no	
1606	U/10	10	6.8	100	yes	no	
1607	U	5	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1608	U	5	7.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1611	U	1	6.8	75	yes	no	
1624	U	12	3.9	75 56	yes	no	1.5 V and 2.1 V Lithium
1625	U/7	5	5.8	75	yes	no	
1626	U	20	5.8	100	yes	no	
1627	U/7	20	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1628	U	20	5.8	75	yes	no	
1629	U/7	5	6.8	75	yes	no	

Where:

U = Chip in trays.
U/7 = Chip with bumps on tape.
U/10 = Chip on foil.
T = SOT144.

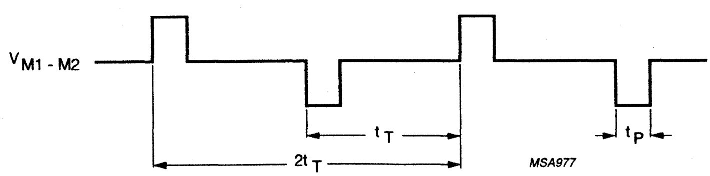
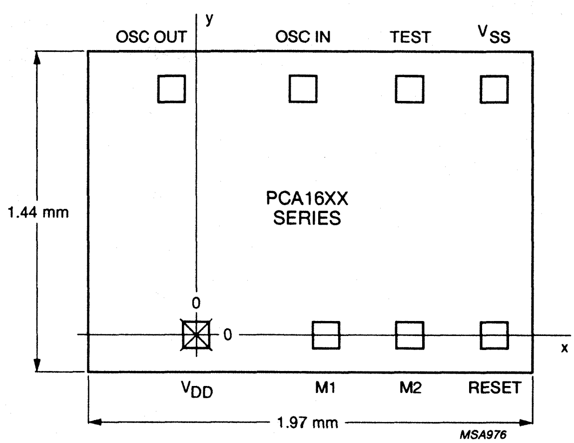


Fig.5 Motor output waveform (normal operation).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 2.84 mm².

Bonding pad dimensions: 110 μm x 110 μm.

Chip thickness: 200 ±25 μm, with bumps: 270 ±25 μm.

Fig.6 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to the center of pad (V_{DD}), see Fig.6.

PAD	X	Y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−495	−170

32 kHz watch circuit using a silver-oxide or a 3 V lithium battery

PCA167X series

FEATURES

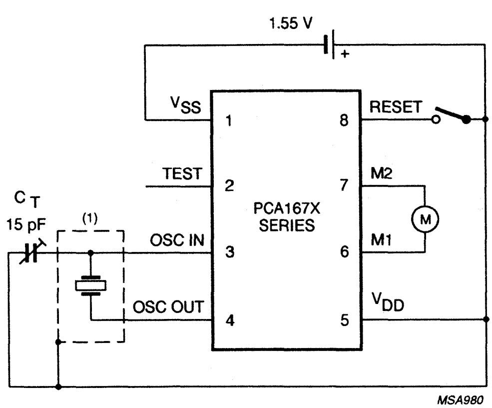
- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Very low current consumption; typically 150 nA
- Stop function for accurate timing
- Chopped motor pulses available
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA167X series are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA167XT	8	micro-flat-pack	plastic	SOT144A
PCA167XU	–	chip in tray	–	–



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

Fig.1 Typical application circuit diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	positive supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

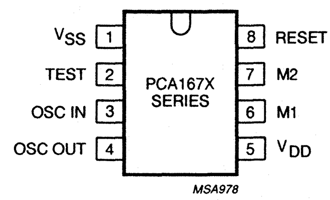


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Motor pulse

The motor output pulse widths (t_P) and the cycle times (t_T) are given in Table 1.

Power-on reset

For correct operation of the power-on reset the rise time of V_{DD} from 0 V to 1.55 V should be less than 0.1 ms. All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing and stop mode

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a HIGH impedance 3-state condition and a 32 Hz signal is produced at the TEST pin. A debounce circuit protects against accidental stoppages due to mechanical shock to the watch (t_{DEB} = 14.7 to 123.2 ms).

Connecting RESET to V_{SS} activates the test mode. The motor pulse period is 31.25 ms instead of t_T. Test and stop mode are disabled by disconnecting RESET (open-circuit).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages	note 2	V_{SS}	V_{DD}	V
	output short-circuit duration		indefinite		
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C
V_{es}	electrostatic handling	note 3	−800	+800	V

Notes

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.
2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').
3. Equivalent to three discharges of a 100 pF capacitor at 800 V, through a resistor of 1.5 kΩ (with positive and negative polarity).

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.5	3.5	V
ΔV_{DD}	supply voltage	transient; V_{DD} = 1.2 to 3.5 V	−	−	0.25	V
I_{DD1}	supply current	between motor pulses	−	150	250	nA
I_{DD2}	supply current	between motor pulses; V_{DD} = 3.5 V	−	200	350	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	−	180	300	nA
I_{DD4}	supply current	stop mode; pin 8 connected to V_{DD}; V_{DD} = 3.5 V	−	300	480	nA
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_L = 2 kΩ; T_{amb} = −10 to +60 °C	−	150	200	mV
R_{sc}	short-circuit resistance Σ (P + N)	$I_{transistor}$ < 1 mA	−	200	300	Ω
t_T	cycle time		note 1			
t_P	pulse width		note 2			
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	−	−	V
g_m	transconductance	$V_{i(p-p)}$ = 50 mV	6	15	−	µS
t_{osc}	start-up time		−	1	−	s
$\Delta f/f$	frequency stability	ΔV_{DD} = 100 mV	−	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		−	3	−	pF
C_o	output capacitance		19	24	29	pF
Reset input						
f_o	output frequency		−	32	−	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	−	−	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	−	1	−	µs
I_{im}	peak input current	note 3	−	320	−	nA
$I_{i(av)}$	average input current		−	10	−	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Test mode						
t_{T1}	cycle time		–	31.25	–	ms
t_{DEB}	debounce time	RESET = V_{DD}	14.7	–	123.2	ms

Notes

1. Cycle time can be changed to one of the following values: 1, 5, 10, 12 or 20 s (see Table 1).
2. Pulse width can be varied from 2 ms to 15.7 ms in steps of 1 ms (see Table 1).
3. Duty factor is 1:32 and RESET = V_{DD} or V_{SS}.

Table 1 Available types and timing information (see Fig.3).

TYPE NUMBER	DELIVERY FORMAT	PERIOD t_T (s)	SPECIFICATIONS				
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS
1672	T	1	7.8	56	no	no	3 V Lithium
1673	U	1	5.8	56	no	no	3 V Lithium
1675	U	1/16	5.8	100	no	no	no oscillator
1676	U/10	10	5.8	56	no	no	3 V Lithium
1677	T	10	7.8	100	no	no	1.5 V

Where:

U = Chip in trays.

U/10 = Chip on foil.

T = SOT144.

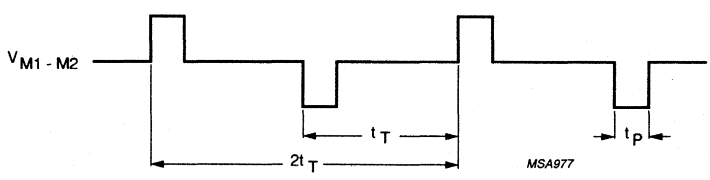
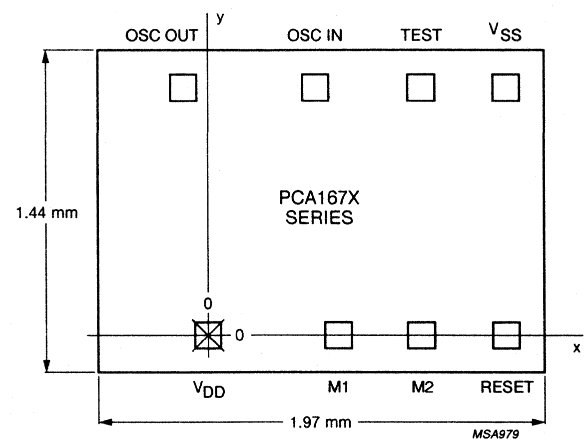


Fig.3 Motor output waveform (normal operation).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 2.84 mm^2.

Bonding pad dimensions: 110 µm x 110 µm.

Chip thickness: 200 ±25 µm, with bumps: 270 ±25 µm.

Fig.4 Bonding pad locations.

Table 2 Bonding pad locations (dimensions in µm).
All x/y coordinates are referenced to the center of pad (V_{DD}), see Fig.4.

PAD	X	Y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	936	0
RESET	1290	0
chip corner (max. value)	−495	−170

4-digit LCD car clock — PCF1171C

FEATURES

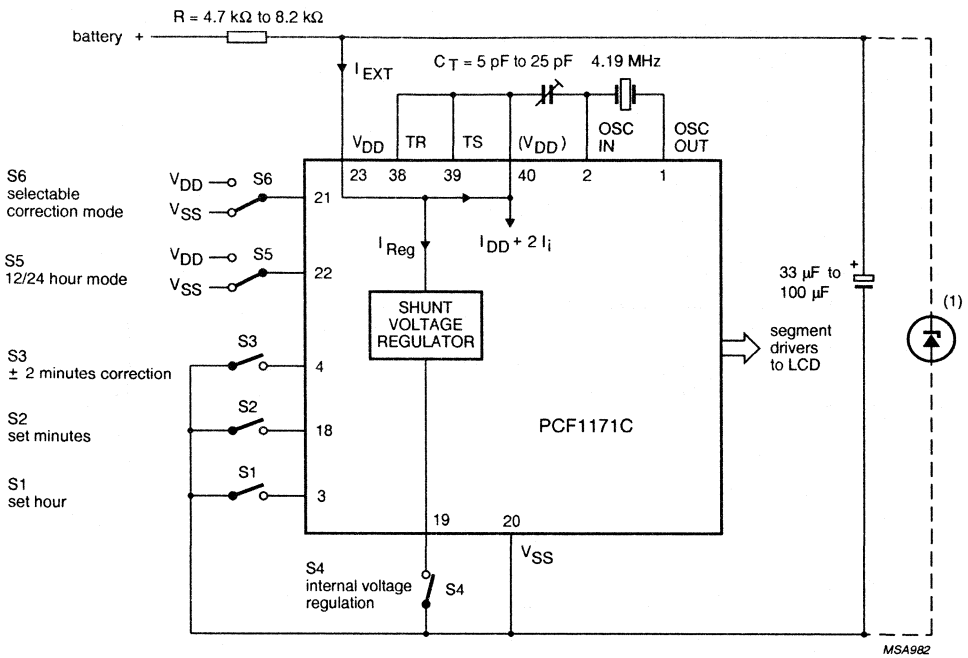
- Driving standard 3½ or a 4-digit LCD
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4.19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature: −40 to +85 °C
- 40-lead plastic mini-pack (VSO40FD).

GENERAL DESCRIPTION

The PCF1171C is a single chip, 4.19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½ or 4-digit liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. A bonding option allows the selection of 12-hour or 24-hour display mode. The circuit is battery-operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1171CT	40	VSO40FD	plastic	SOT158B
PCF1171CU	–	uncased chip in tray	–	–



(1) Only required if internal regulation is disconnected.

From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

Fig.1 Typical application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC OUT	1	oscillator output
OSC IN	2	oscillator input
S1	3	set hour
S3	4	±2 minute correction
BP	5	64 Hz backplane driver (common of LCD)
ADEG1	6	segment driver
C1	7	segment driver
E2	8	segment driver
D2	9	segment driver
C2	10	segment driver
E3	11	segment driver
D3	12	segment driver
C3	13	segment driver
E4	14	segment driver
D4	15	segment driver
C4	16	segment driver
B4	17	segment driver
S2	18	set minutes
S4	19	internal voltage regulation
V_{SS}	20	negative supply
S6	21	selectable correction mode
S5	22	12/24-hour mode
V_{DD}	23	positive supply
A4	24	segment driver
F4	25	segment driver
G4	26	segment driver
B3	27	segment driver
A3	28	segment driver
F3	29	segment driver
G3	30	segment driver
P1,P2	31	colon flashing
P3,P4	32	colon static
B2	33	segment driver
A2	34	segment driver
F2	35	segment driver
G2	36	segment driver
B1	37	segment driver
TR	38	test reset; connect to (V_{DD})
TS	39	test speed-up; connect to (V_{DD})
(V_{DD})	40	positive supply for test and oscillator inputs

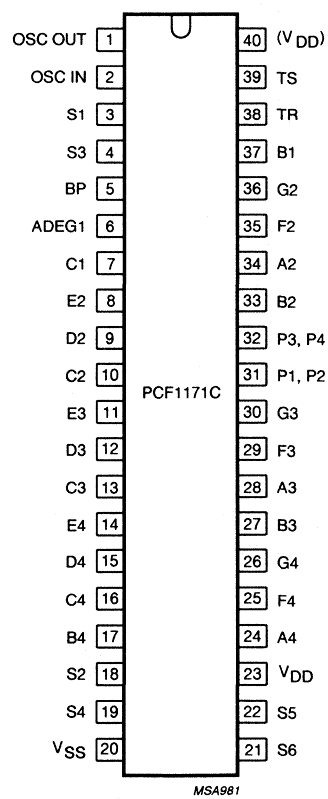


Fig.2 Pin configuration.

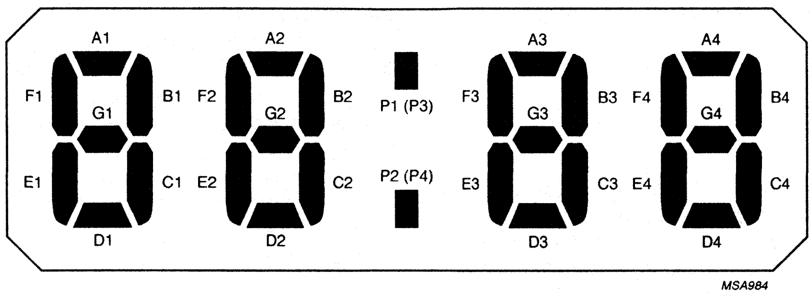


Fig.3 Segment designation of LCD.

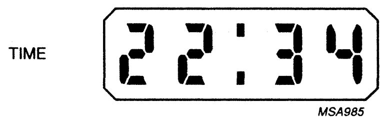


Fig.4 Display mode.

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

SWITCH S1

Set hours, S6 selects mode of correction.

SWITCH S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

SWITCHES S1 AND S2

Segment test: if S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00 in the 12-hour mode or 0 : 00 in the 24-hour mode.

Switch options

SWITCH S3

Time correction ±2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

SWITCH S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open, the circuit has to be supplied with an externally regulated voltage.

SWITCH S5

12-hour display mode: S5 is connected to V_{DD} for 12-hour operation.
24-hour display mode: S5 is connected to V_{SS} for 24-hour operation.

SWITCH S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65 536. In this mode the maximum input frequency is 100 kHz (external generator at OSC IN). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

Switch functions also operate in the test mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage with respect to V_{SS} with internal regulaton disconnected;	note 1	–	8	V
V_{n-20}	voltage range (any pin)		V_{SS}–0.3	V_{DD}+0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHARACTERISTICS

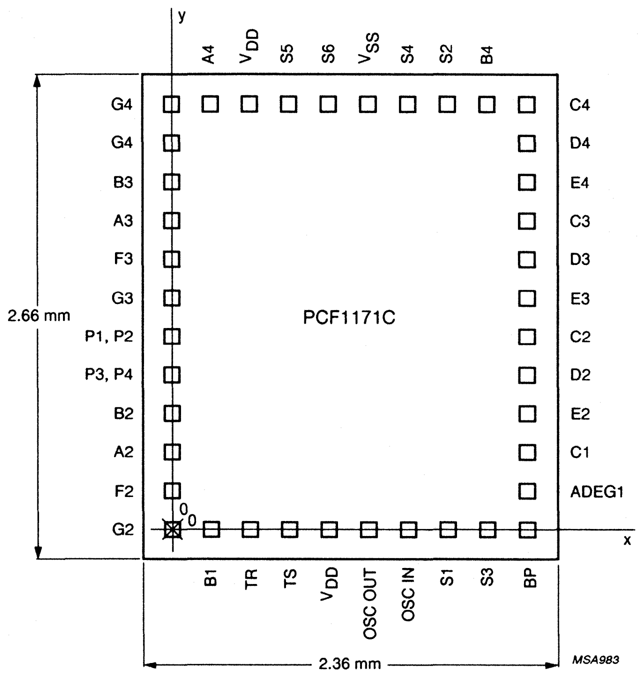
V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	external regulation		3	–	6	V
	internal regulation	I_{REG} = 1 mA	4	5	6	V
I_{REG}	regulation current with internal regulation		0.2	–	5	mA
I_{DD}	current consumption	all switches open; without LCD; internal regulation disconnected; note 1	50	400	700	µA
r_o	differential internal impedance	I_{REG} = 1 mA	–	–	150	Ω
Oscillator (pins 1 and 2; note 2)						
t_{osc}	start time		–	–	200	ms
$\Delta f/f_{osc}$	frequency stability	ΔV_{DD} = 100 mV	–	0.2 x 10^{-6}	1 x 10^{-6}	
R_{fb}	feedback resistance		0.1	–	1	MΩ
C_i	input capacitance		–	–	9	pF
C_o	output capacitance		19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4) and test inputs, TS, TR (pins 38 and 39)						
I_i	input current	with inputs connected to V_{SS}	50	150	500	µA
t_d	debounce time		32	–	150	ms
R_S	segment driver output resistance	I_L = ±50 µA	–	1	2.5	kΩ
R_{BP}	backplane driver output resistance	I_L = ±250 µA	–	0.2	0.5	kΩ
f_{BP}	backplane driver output frequency		–	64	–	Hz
	LCD DC offset voltage	R_L = 200 kΩ; C_L = 1 nF	–	–	±50	mV

Notes

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$ (+ LCD current).
2. For correct operation of the oscillator: $V_{DD} \geq 3$ V.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6.28 mm^2.

Bonding pad dimensions: 110 μm x 110 μm.

Chip thickness: 381 ±25 μm.

Fig.5 Bonding pad locations; 40 terminals.

Table 1 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to the pad G2, see Fig.5.

PAD	X	Y	PAD	X	Y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	S5	660	2320
S1	1460	0	V_{DD}	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
ADEG1	1920	240	G4	0	2080
C1	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1,P2	0	1060
D3	1920	1460	P3,P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V_{SS}	1060	2320	V_{DD}	860	0
chip corner (max. value)	−220	−170			

3½-digit LCD car clock PCF1172C

FEATURES

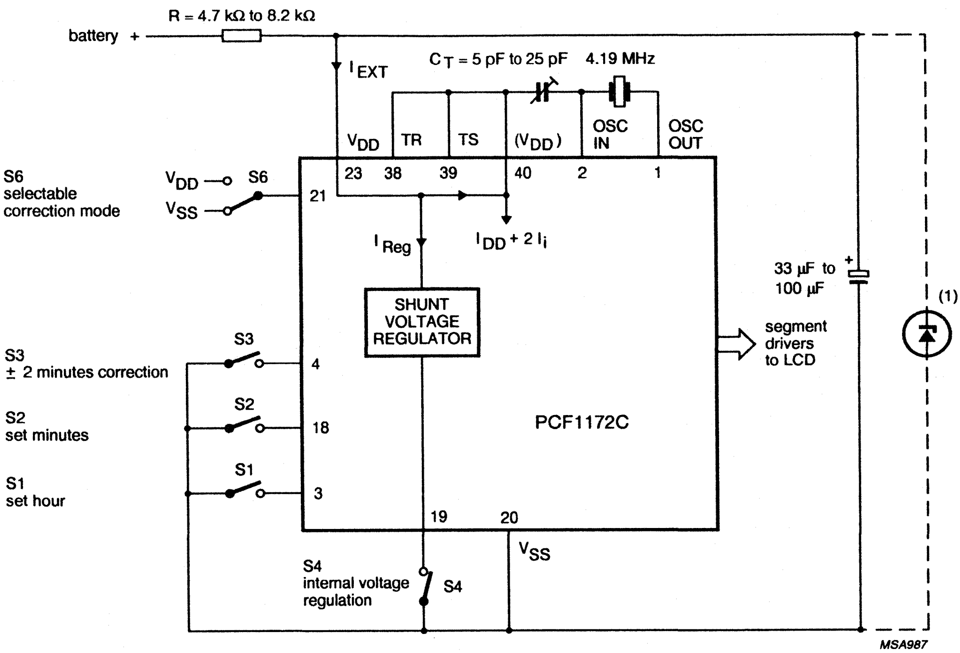
- Driving standard 3½-digit LCD with AM and PM indicators
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4.19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature: −40 to +85 °C
- 40-lead plastic mini-pack (VSO40FD).

GENERAL DESCRIPTION

The PCF1172C is a single chip, 4.19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½-digit liquid crystal display (LCD) with AM and PM indicators. Two single-pole, single-throw switches accomplish all time setting functions. The circuit is battery-operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1172CT	40	VSO40FD	plastic	SOT158B
PCF1172CU	–	uncased chip in tray	–	–



(1) Only required if internal regulation is disconnected.

From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

Fig.1 Typical application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC OUT	1	oscillator output
OSC IN	2	oscillator input
S1	3	set hour
S3	4	±2 minute correction
BP	5	64 Hz backplane driver (common of LCD)
PM	6	segment output for PM annunciator
AM	7	segment output for AM annunciator
E2	8	segment driver
D2	9	segment driver
C2	10	segment driver
E3	11	segment driver
D3	12	segment driver
C3	13	segment driver
E4	14	segment driver
D4	15	segment driver
C4	16	segment driver
B4	17	segment driver
S2	18	set minutes
S4	19	internal voltage regulation
V_{SS}	20	negative supply
S6	21	selectable correction mode
n.c.	22	not connected
V_{DD}	23	positive supply
A4	24	segment driver
F4	25	segment driver
G4	26	segment driver
B3	27	segment driver
A3	28	segment driver
F3	29	segment driver
G3	30	segment driver
P1,P2	31	colon flashing
P3,P4	32	colon static
B2	33	segment driver
A2	34	segment driver
F2	35	segment driver
G2	36	segment driver
B1,C1	37	segment driver
TR	38	test reset; connect to (V_{DD})
TS	39	test speed-up; connect to (V_{DD})
(V_{DD})	40	positive supply for test and oscillator inputs

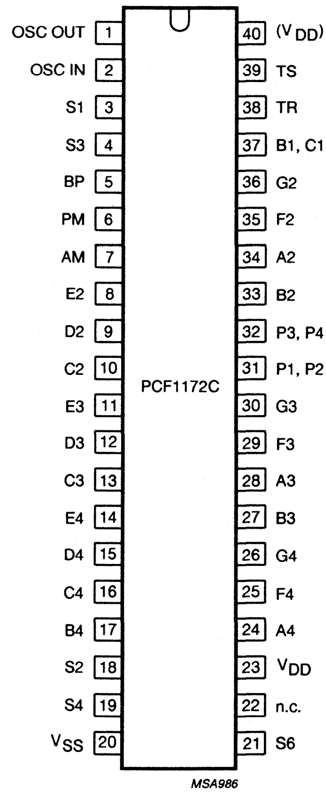


Fig.2 Pin configuration.

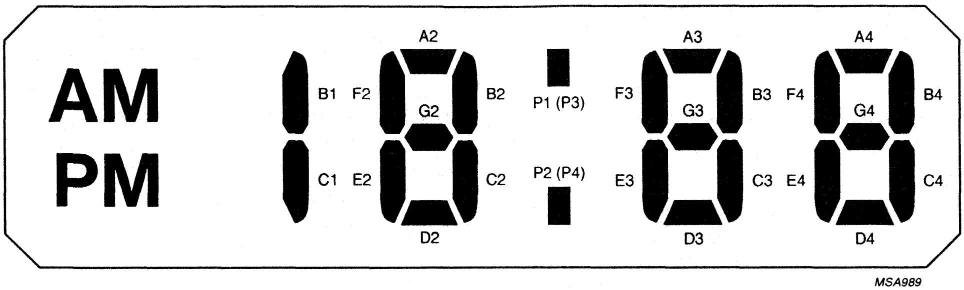


Fig.3 Segment designation of LCD.

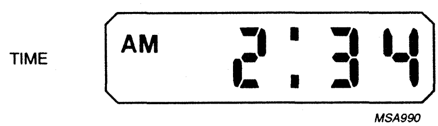


Fig.4 12-hour display mode.

SWITCH FUNCTIONS

Time set mode

Switch inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of single-pole, single-throw contacts. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

SWITCH S1

Set hours, S6 selects mode of correction.

SWITCH S2

Set minutes, S6 selects mode of correction. When S2 is closed, in addition to the minute correction, the second counter is set to zero. Release of S2 sets the second counter running.

SWITCHES S1 AND S2

Segment test: if S1 and S2 are pressed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00.

Switch options

SWITCH S3

Time correction ±2 minutes, only operates between 58 minutes 00 seconds and 1 minute 59 seconds. By pressing S3 the clock resets to the full hour with minutes and seconds at zero.

SWITCH S4

Internal regulation: S4 is closed; the internal voltage regulator is active and the voltage supply for the LCD is 5 V.
External regulation: S4 is open, the circuit has to be supplied with an externally regulated voltage.

SWITCH S6

Single set correction mode: S6 is connected to V_{DD}; each closure of S1 or S2 advances the counter by one.
Continuous set correction mode: S6 is connected to V_{SS}; each closure of S1 or S2 advances the counter by one and after one second continues with one advance per second until S1 or S2 is released.

Testing

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65 536. In this mode the maximum input frequency is 100 kHz (external generator at OSC IN). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

Switch functions also operate in the test mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage with respect to V_{SS} with internal regulaton disconnected	note 1	–	8	V
$V_{n\text{-}20}$	voltage range (any pin)		V_{SS}–0.3	V_{DD}+0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

CHARACTERISTICS

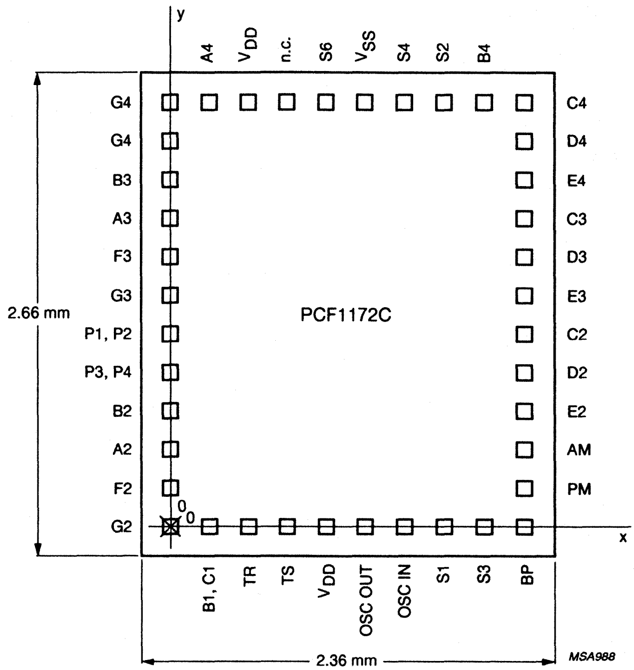
V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	external regulation	3	–	6	V
	external regulation		3	–	6	V
	internal regulation	I_{REG} = 1 mA	4	5	6	V
I_{REG}	regulation current with internal regulation		0.2	–	5	mA
I_{DD}	current consumption	all switches open; without LCD; internal regulation disconnected; note 1	50	400	700	µA
r_o	differential internal impedance	I_{REG} = 1 mA	–	–	150	Ω
Oscillator (pins 1 and 2; note 2)						
t_{osc}	start time		–	–	200	ms
$\Delta f/f_{osc}$	frequency stability	ΔV_{DD} = 100 mV	–	0.2×10^{-6}	1×10^{-6}	
R_{fb}	feedback resistance		0.1	–	1	MΩ
C_i	input capacitance		–	–	9	pF
C_o	output capacitance		19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4)						
I_i	input current	with inputs connected to V_{SS}	50	150	500	µA
t_d	debounce time		32	–	150	ms
R_S	segment driver output resistance	I_L = ±50 µA	–	1	2.5	kΩ
R_{BP}	backplane driver output resistance	I_L = ±250 µA	–	0.2	0.5	kΩ
f_{BP}	backplane driver output frequency		–	64	–	Hz
	LCD DC offset voltage	R_L = 200 kΩ; C_L = 1 nF	–	–	±50	mV

Notes

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$.
2. For correct operation of the oscillator: $V_{DD} \geq 3$ V.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



n.c. = not connected.

Chip area: 6.28 mm^2.

Bonding pad dimensions: 110 μm x 110 μm.

Chip thickness: 381 ±25 μm.

Fig.5 Bonding pad locations; 40 terminals.

Table 1 Bonding pad locations (dimensions in µm).
All x/y coordinates are referenced to the pad G2, see Fig.5.

PAD	X	Y	PAD	X	Y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	n.c.	660	2320
S1	1460	0	V_{DD}	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
PM	1920	240	G4	0	2080
AM	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1,P2	0	1060
D3	1920	1460	P3,P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1,C1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V_{SS}	1060	2320	V_{DD}	860	0
chip corner (max. value)	−220	−170			

4-digit static LCD car clock | PCF1174C

FEATURES

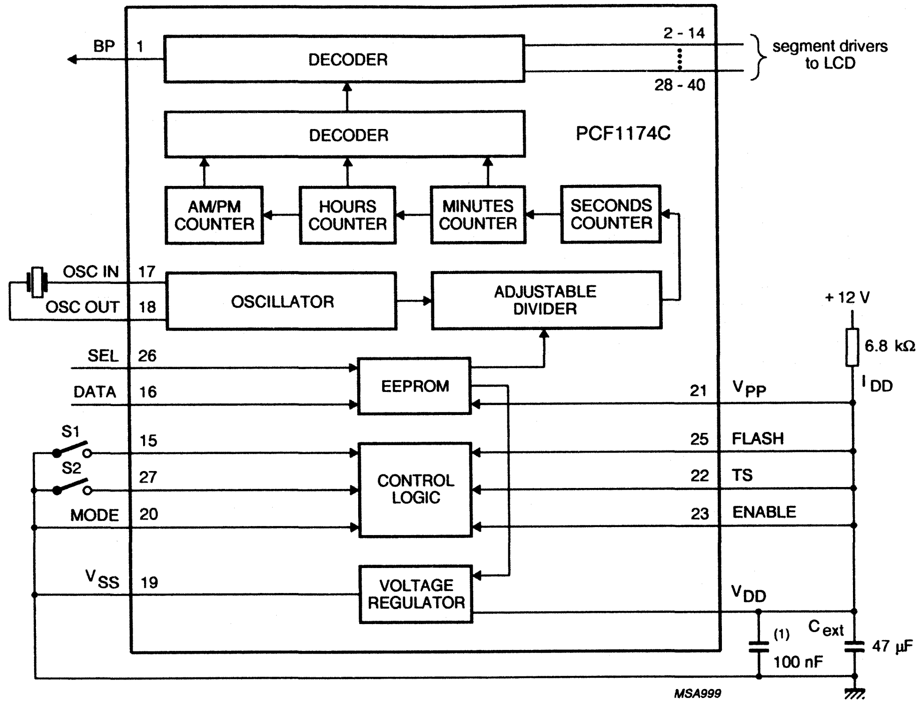
- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: −40 to +85 °C
- 40-lead plastic mini-pack (VSO40FD).

GENERAL DESCRIPTION

The PCF1174C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit static liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1174CT	40	VSO40FD	plastic	SOT158B
PCF1174CU	–	uncased chip in tray	–	–



(1) To be placed close to the IC.

Fig.1 Typical application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BP	1	backplane output
PM	2	segment driver
AM	3	segment driver
ADEG1	4	segment driver
C1	5	segment driver
E2	6	segment driver
D2	7	segment driver
C2	8	segment driver
E3	9	segment driver
C3	10	segment driver
E4	11	segment driver
D4	12	segment driver
C4	13	segment driver
B4	14	segment driver
S1	15	hour adjustment input
DATA	16	EEPROM data input
OSC IN	17	oscillator input
OSC OUT	18	oscillator output
V_{SS}	19	negative supply
MODE	20	12/24-hour mode select input
V_{PP}	21	programming voltage input
TS	22	test speed-up mode input
ENABLE	23	set enable input for S1 and S2
V_{DD}	24	positive supply voltage
FLASH	25	colon option input
SEL	26	EEPROM select input
S2	27	minute adjustment input
A4	28	segment driver
F4	29	segment driver
G4	30	segment driver
B3	31	segment driver
AD3	32	segment driver
F3	33	segment driver
G3	34	segment driver
COL	35	segment driver
B2	36	segment driver
A2	37	segment driver
F2	38	segment driver
G2	39	segment driver
B1	40	segment driver

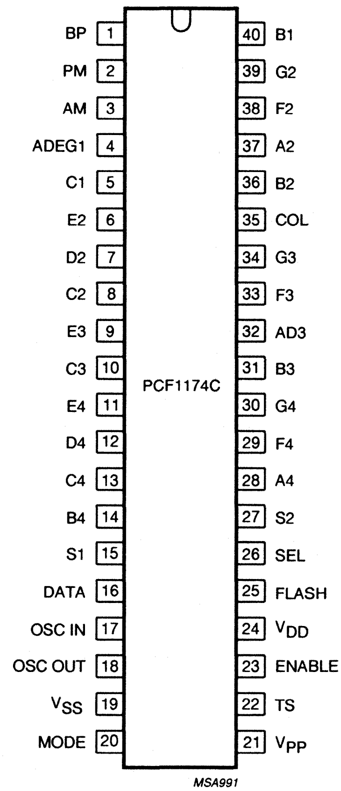


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs static data to the LCD. Generation of BP and the output signals are shown in Fig.5.

The average voltages across the segments are:

$V_{ON(RMS)} = V_{DD}$

$V_{OFF(RMS)} = 0\ V.$

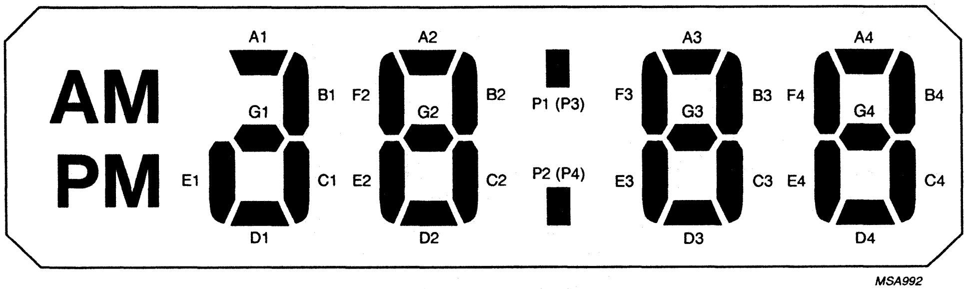


Fig.3 Segment designation of LCD.

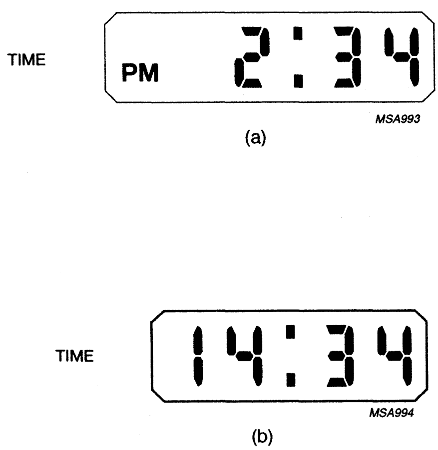


Fig.4 Typical displays; (a) 12-hour mode, (b) 24-hour mode.

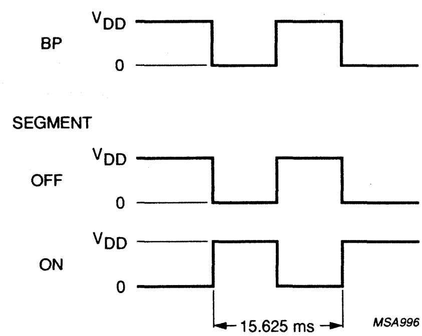


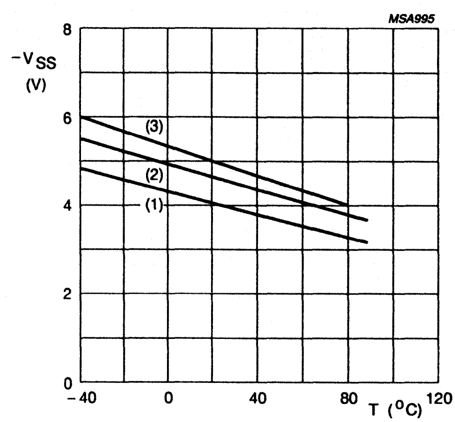
Fig.5 Backplane and output signals.

LCD voltage (Fig.6)

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast, e.g. when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C

V_{DD} = 5 to 6 V at –40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.6 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM;	12-hour mode
0:00;	24-hour mode.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation +60 ppm) by capacitors at the oscillator input and output, a number (n) of 262144 Hz are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.7):

1. Set SEL to V_{SS} and a level of V_{DD} – 5 V to V_{PP}.
2. The quartz-frequency deviation Δf/f is measured and (n) is calculated (see Table 1).
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency.
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and when correct fixed by applying the store pulse t_W.
6. Release SEL and V_{PP}.

Table 1 Time calibration (Δt = 3.81 µs; SEL at V_{SS}).

OSCILLATOR-FREQUENCY DEVIATION Δf/f (ppm)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.629
+7.6	2	15.633
+11.4	3	15.636
.	.	.
.	.	.
.	.	.
+117.8	31	15.743

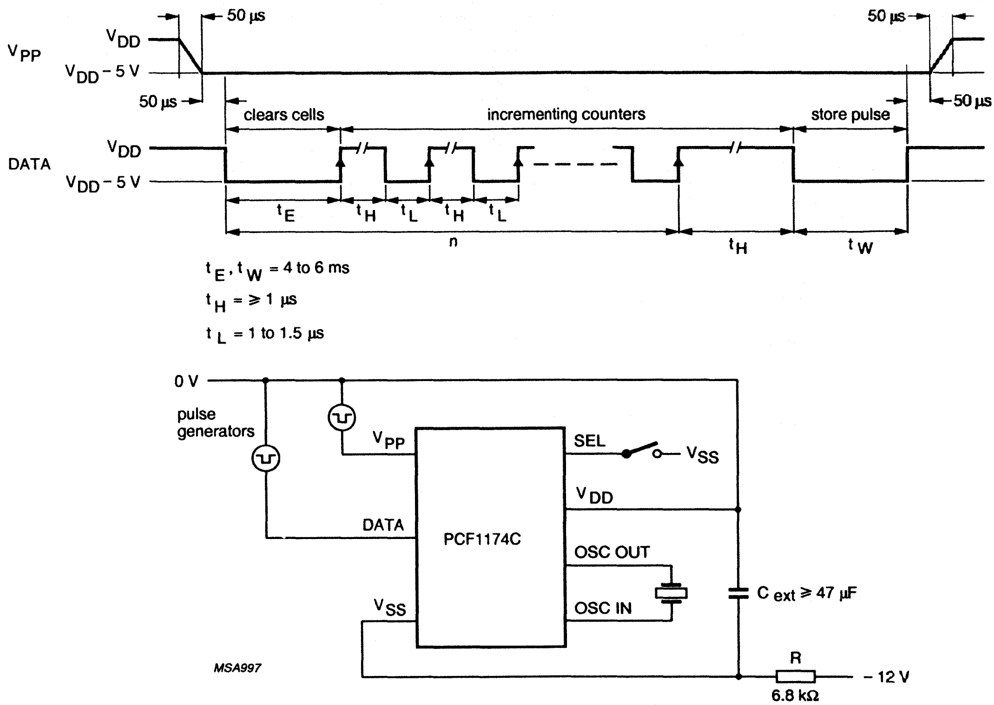


Fig.7 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	voltage range	all pins except V_{PP} and DATA	–0.3	V_{DD}+0.3	V
		pins V_{PP} and DATA	–3	V_{DD}+0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

Handling MOS devices

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

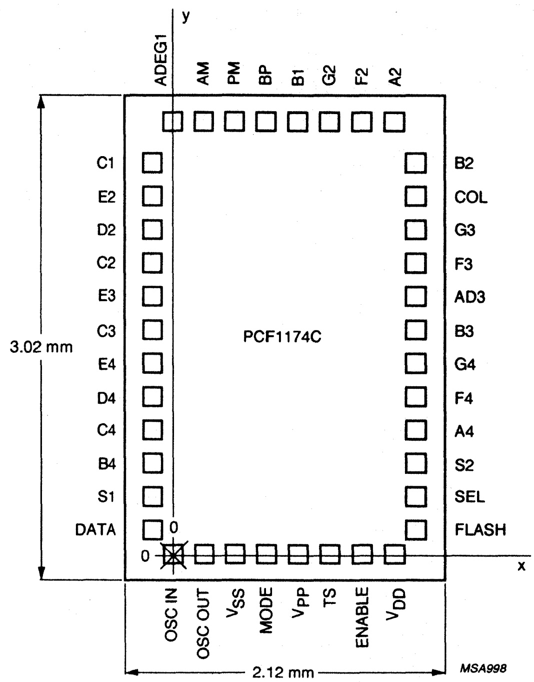
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ±30 x 10^{-6}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	−0.35	–	%/K
		V_{DD} = 4.5 V	–	−16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	μA
C_{EXT}	capacitance	external capacitor	47	–	–	μF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60 x 10^{-6}	110 x 10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1 x 10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
I_{IL}	leakage current	FLASH, ENABLE, MODE	–	–	2	μA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	V_{PP} = V_{DD} − 5 V	70	–	700	μA
		during programming	–	500	–	μA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 μA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 μA	–	–	5	kΩ
LCD						
V_{DC}	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   V_{DD} = 5 V; R max. (12 V − 5 V)/700 μA = 10 kΩ;
   V_{DD} = 5 V; R typ. (12 V − 5 V)/900 μA = 7.8 kΩ (more reserve);
   I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6.4 mm².

Bonding pad dimensions: 110 µm x 110 µm.

Chip thickness: 381 ±25 µm.

Fig.8 Bonding pad locations.

Table 2 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to the bottom left pad (OSC IN), see Fig.8.

PAD	X	Y	PAD	X	Y
BP	600	2676	V_{PP}	800	0
PM	400	2676	TS	1000	0
AM	200	2676	ENABLE	1200	0
ADEG1	0	2676	V_{DD}	1400	0
C1	−138	2448	FLASH	1538	168
E2	−138	2228	SEL	1538	388
D2	−138	2008	S2	1538	608
C2	−138	1808	A4	1538	808
E3	−138	1608	F4	1538	1008
C3	−138	1408	G4	1538	1208
E4	−138	1208	B3	1538	1408
D4	−138	1008	AD3	1538	1608
C4	−138	808	F3	1538	1808
B4	−138	608	G3	1538	2008
S1	−138	388	COL	1538	2208
DATA	−138	168	B2	1538	2448
OSC IN	0	0	A2	1400	2676
OSC OUT	200	0	F2	1200	2676
V_{SS}	400	0	G2	1000	2676
MODE	600	0	B1	800	2676
chip corner (max. value)	−360	−170			

4-digit duplex LCD car clock PCF1175C

FEATURES

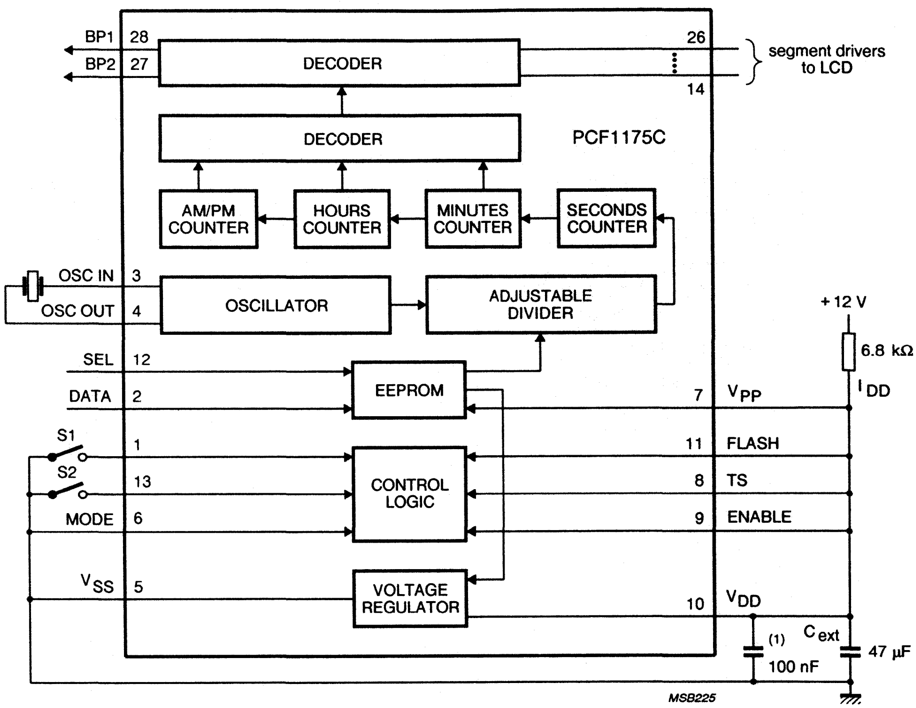
- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 28-lead plastic mini-pack.

GENERAL DESCRIPTION

The PCF1175C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1175CT	28	SO28L	plastic	SOT136A
PCF1175CU	–	uncased chip in tray	–	–
PCF1175CU/10	–	chip-on-film frame carrier (FFC)	–	–



(1) To be placed close to the IC.

Fig.1 Typical application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S1	1	hour adjustment input
DATA	2	EEPROM data input
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{SS}	5	negative supply voltage
MODE	6	12/24-hour mode select input
V_{PP}	7	programming voltage input
TS	8	test speed-up mode input
ENABLE	9	enable input (for S1 and S2)
V_{DD}	10	positive supply voltage
FLASH	11	colon option input
SEL	12	EEPROM select input
S2	13	minute adjustment input
B4/C4	14	segment driver
G4/D4	15	segment driver
F4/E4	16	segment driver
B3/C3	17	segment driver
G3/AD3	18	segment driver
F3/E3	19	segment driver
A4/COL	20	segment driver
B2/C2	21	segment driver
G2/D2	22	segment driver
F2/E2	23	segment driver
B1/C1	24	segment driver
A2/ADEG1	25	segment driver
AM/PM	26	segment driver
BP2	27	backplane 2
BP1	28	backplane 1

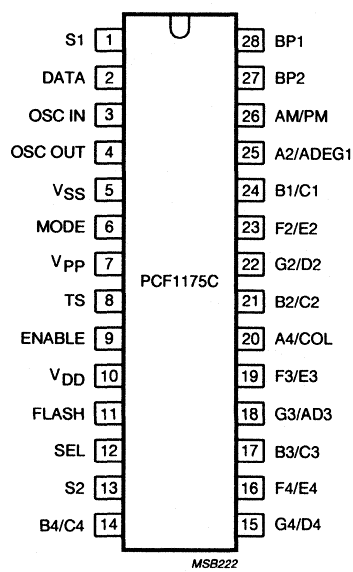


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1:2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.5.

The average voltages across the segments are:

$V_{ON(RMS)} = 0.79V_{DD}$

$V_{OFF(RMS)} = 0.35V_{DD}$.

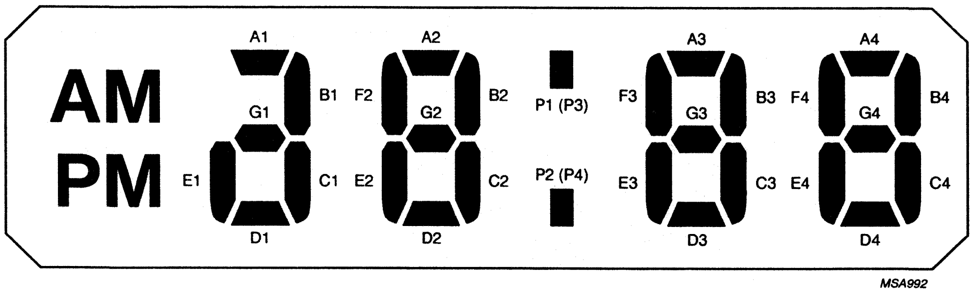


Fig.3 Segment designation of LCD.

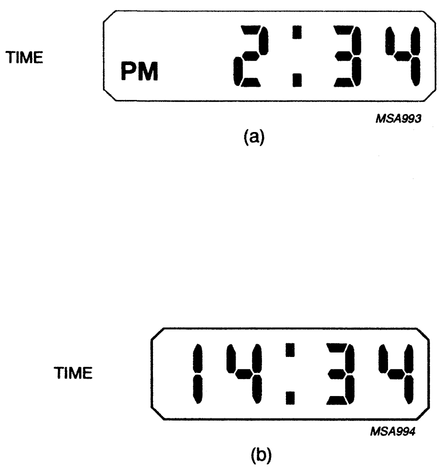


Fig.4 Typical displays; (a) 12-hour mode, (b) 24-hour mode.

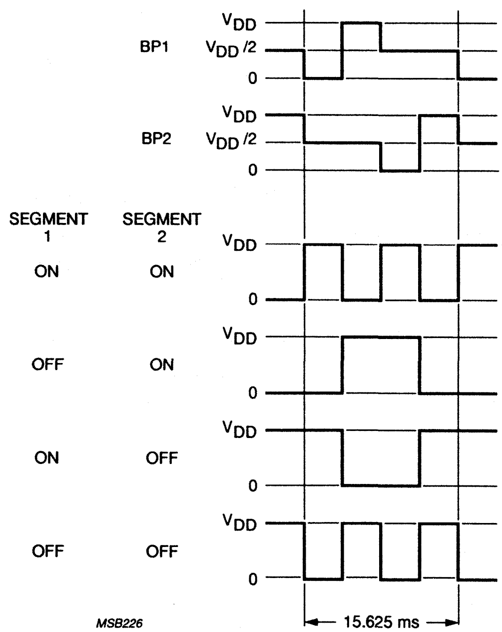


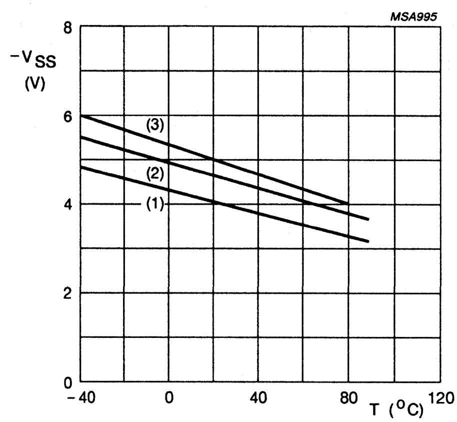
Fig.5 Backplane and output signals.

LCD voltage (Fig.6)

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast, e.g. when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C

V_{DD} = 5 to 6 V at –40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).

(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).

(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.6 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

MODE connected to V_{DD}:	12-hour mode,	1:00 AM
MODE connected to V_{SS}:	24-hour mode,	0:00
MODE left open-circuit:	24-hour mode,	0:00 or 1:00.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation +60 ppm) by capacitors at the oscillator input and output, a number (n) of 262144 Hz are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.7):

1. Set SEL to V_{SS} and a level of V_{DD} – 5 V to V_{PP}.
2. The quartz-frequency deviation Δf/f is measured and (n) is calculated (see Table 1).
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency.
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and when correct fixed by applying the store pulse t_W.
6. Release SEL and V_{PP}.

Table 1 Time calibration (Δt = 7.63 µs; SEL at V_{SS}).

OSCILLATOR-FREQUENCY DEVIATION Δf/f (ppm)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.633
+7.6	2	15.641
+11.4	3	15.648
.	.	.
.	.	.
.	.	.
+117.8	31	15.861

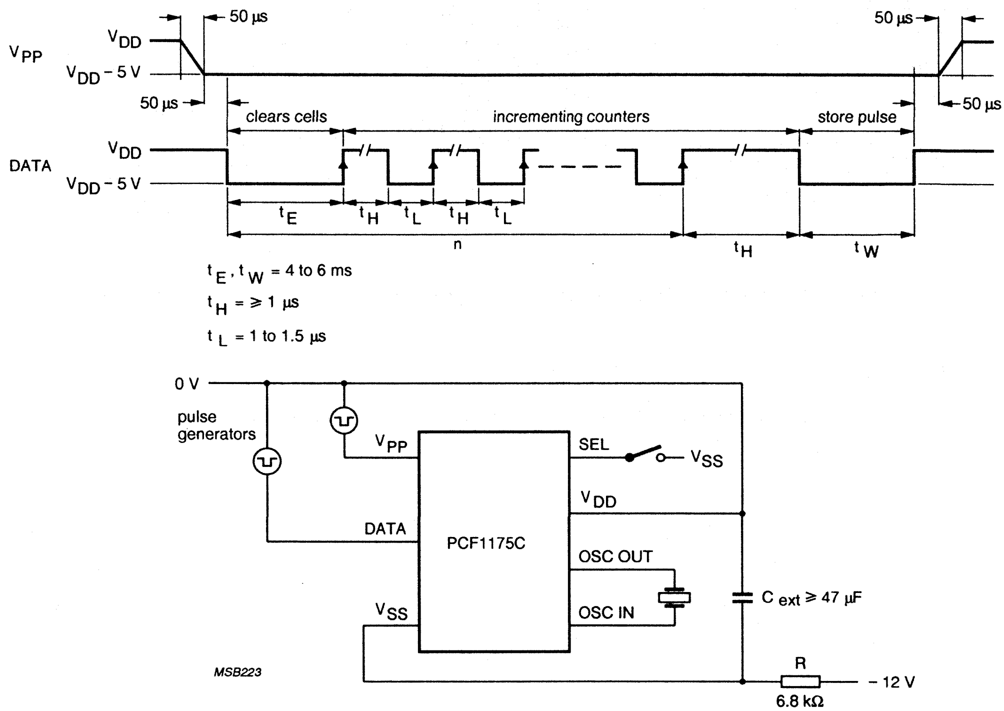


Fig.7 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	voltage range	all pins except V_{PP} and DATA	–0.3	V_{DD}+0.3	V
		pins V_{PP} and DATA	–3	V_{DD}+0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

Handling MOS devices

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

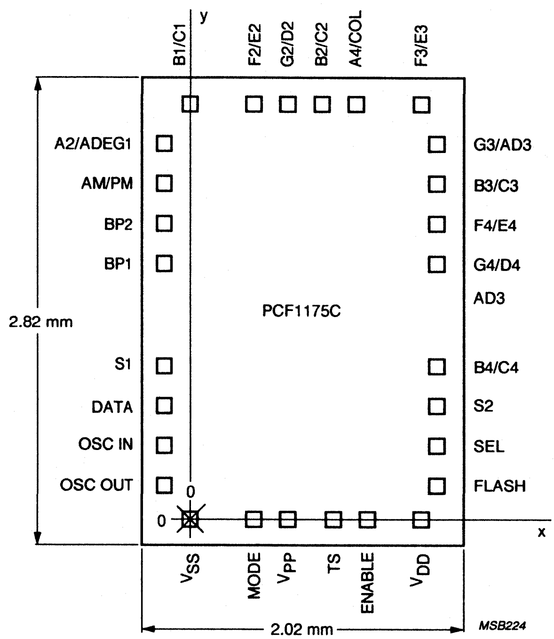
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ±30 x 10^{-6}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	−0.35	–	%/K
		V_{DD} = 4.5 V	–	−16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	µA
C_{EXT}	capacitance	external capacitor	47	–	–	µF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60 x 10^{-6}	110 x 10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1 x 10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
R_O	pull-up/pull-down resistance	MODE	100	300	1000	kΩ
I_{IL}	leakage current	ENABLE, FLASH	–	–	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD} - 5$ V	70	–	700	µA
		during programming	–	500	–	µA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 µA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	–	–	5	kΩ
LCD						
V_{DC}	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   V_{DD} = 5 V; R max. (12 V − 5 V)/700 µA = 10 kΩ;
   V_{DD} = 5 V; R typ. (12 V − 5 V)/900 µA = 7.8 kΩ (more reserve);
   I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.69 mm².

Bonding pad dimensions: 110 µm x 110 µm.

Chip thickness: 381 ±25 µm.

Fig.8 Bonding pad locations.

Table 2 Bonding pad locations (dimensions in μm).
All x/y coordinates are referenced to the bottom left pad (V_{SS}), see Fig.8.

PAD	X	Y	PAD	X	Y
S1	−138	881	G4/D4	1438	1588
DATA	−138	639	F4/E4	1438	1808
OSC IN	−138	408	B3/C3	1438	2028
OSC OUT	−138	188	G3/AD3	1438	2248
V_{SS}	0	0	F3/E3	1400	2476
MODE	383	0	A4/COL	1000	2476
V_{PP}	583	0	B2/C2	800	2476
TS	846	0	G2/D2	600	2476
ENABLE	1046	0	F2/E2	400	2476
V_{DD}	1352	0	B1/C1	0	2476
FLASH	1438	188	A2/ADEG1	−138	2248
SEL	1438	408	AM/PM	−138	2028
S2	1438	628	BP2	−138	1808
B4/C4	1438	848	BP1	−138	1588
chip corner (max. value)	−360	−170			

4-digit duplex LCD car clock PCF1178C

FEATURES

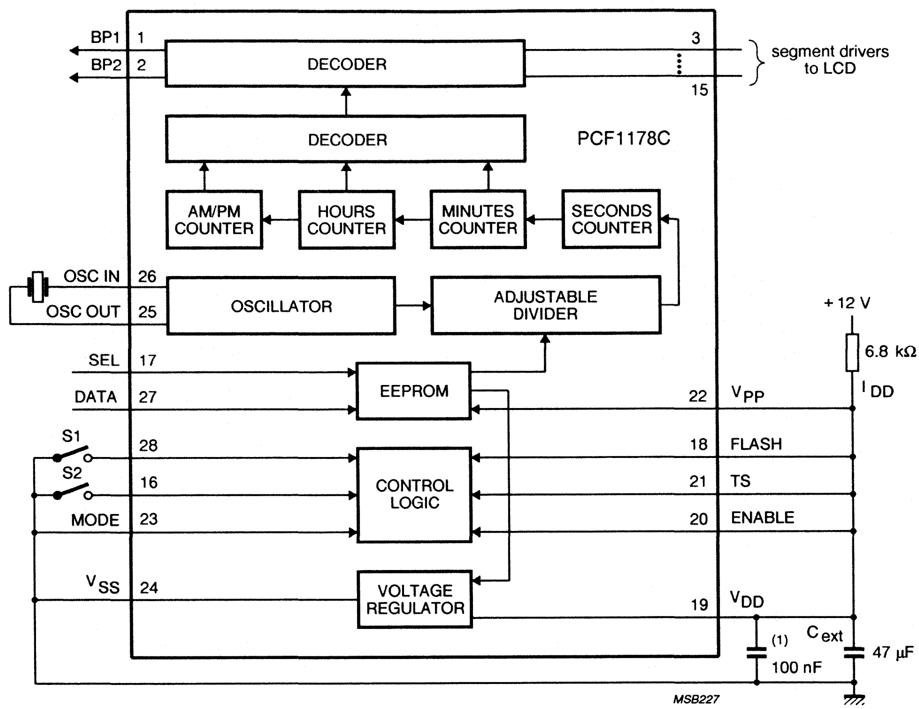
- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: −40 to +85 °C
- 28-lead plastic mini-pack.

GENERAL DESCRIPTION

The PCF1178C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1178CT	28	SO28L	plastic	SOT136A
PCF1178CU	–	uncased chip in tray	–	–
PCF1178CU/10	–	chip-on-film frame carrier (FFC)	–	–
PCF1178CU/5	–	unsawn wafer	–	–



(1) To be placed close to the IC.

Fig.1 Typical application diagram.

4-digit duplex LCD car clock PCF1178C

PINNING

SYMBOL	PIN	DESCRIPTION
BP1	1	backplane 1
BP2	2	backplane 2
AM/PM	3	segment driver
A2/ADEG1	4	segment driver
B1/C1	5	segment driver
F2/E2	6	segment driver
G2/D2	7	segment driver
B2/C2	8	segment driver
A4/COL	9	segment driver
F3/E3	10	segment driver
G3/AD3	11	segment driver
B3/C3	12	segment driver
F4/E4	13	segment driver
G4/D4	14	segment driver
B4/C4	15	segment driver
S2	16	minute adjustment input
SEL	17	EEPROM select input
FLASH	18	colon option input
V_{DD}	19	positive supply voltage
ENABLE	20	enable input (for S1 and S2)
TS	21	test speed-up mode input
V_{PP}	22	programming voltage input
MODE	23	12/24-hour mode select input
V_{SS}	24	negative supply voltage
OSC OUT	25	oscillator output
OSC IN	26	oscillator input
DATA	27	EEPROM data input
S1	28	hour adjustment input

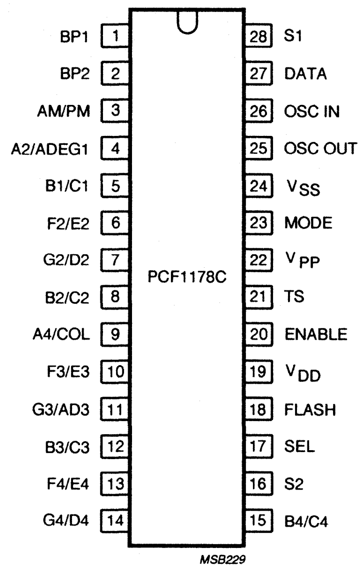


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1:2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.5.

The average voltages across the segments are:

$V_{ON(RMS)} = 0.79V_{DD}$

$V_{OFF(RMS)} = 0.35V_{DD}$.

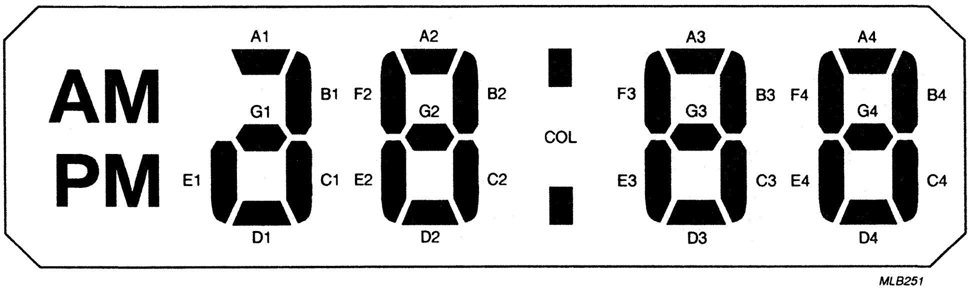


Fig.3 Segment designation of LCD.

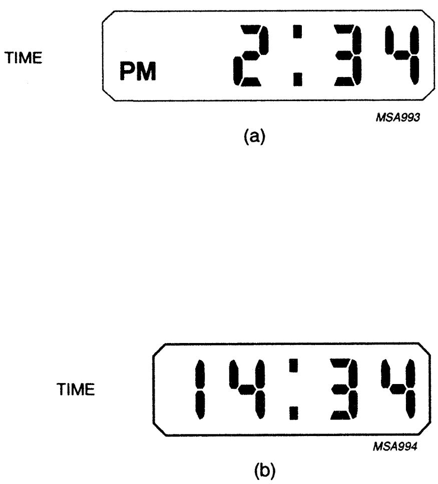


Fig.4 Typical displays; (a) 12-hour mode, (b) 24-hour mode.

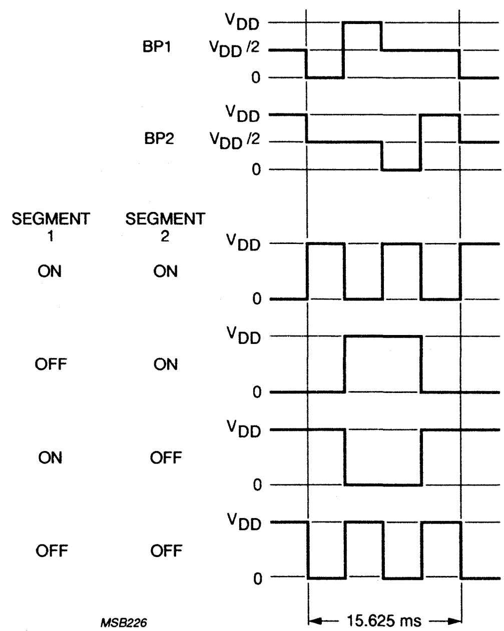


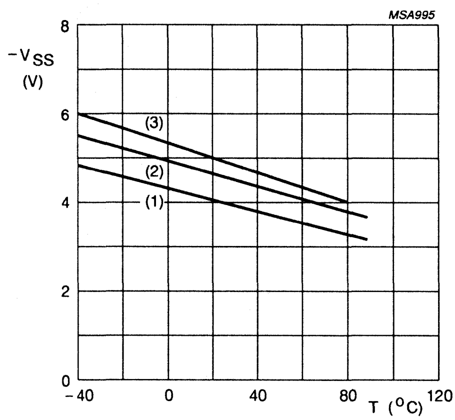
Fig.5 Backplane and output signals.

LCD voltage (Fig.6)

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast, e.g. when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C

V_{DD} = 5 to 6 V at −40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.6 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

MODE connected to V_{DD}:	12-hour mode,	1:00 AM
MODE connected to V_{SS}:	24-hour mode,	0:00
MODE left open-circuit:	24-hour mode,	0:00 or 1:00.

Colon

If FLASH is connected to V_{DD} the colon pulses at 0.5 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with two advances per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation +60 ppm) by capacitors at the oscillator input and output, a number (n) of 262144 Hz are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.7):

1. Set SEL to V_{SS} and a level of V_{DD} – 5 V to V_{PP}.
2. The quartz-frequency deviation Δf/f is measured and (n) is calculated (see Table 1).
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency.
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and when correct fixed by applying the store pulse t_W.
6. Release SEL and V_{PP}.

Table 1 Time calibration (Δt = 7.63 µs; SEL at V_{SS}).

OSCILLATOR-FREQUENCY DEVIATION Δf/f (ppm)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.633
+7.6	2	15.641
+11.4	3	15.648
.	.	.
.	.	.
.	.	.
+117.8	31	15.861

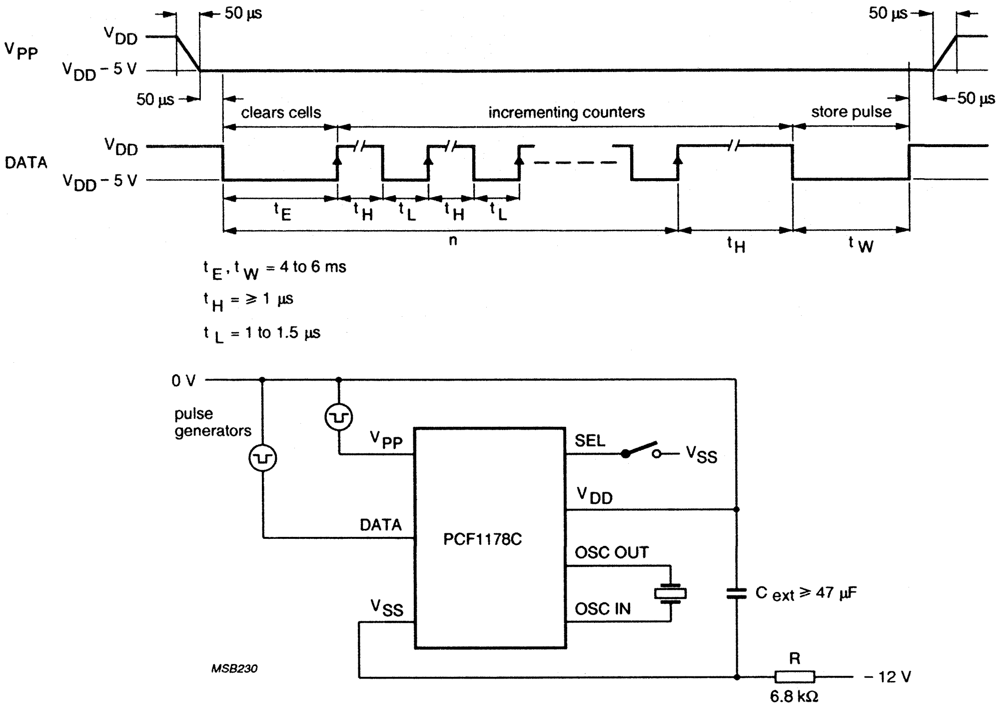


Fig.7 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	voltage range	all pins except V_{PP} and DATA	−0.3	V_{DD}+0.3	V
		pins V_{PP} and DATA	−3	V_{DD}+0.3	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

Handling MOS devices

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

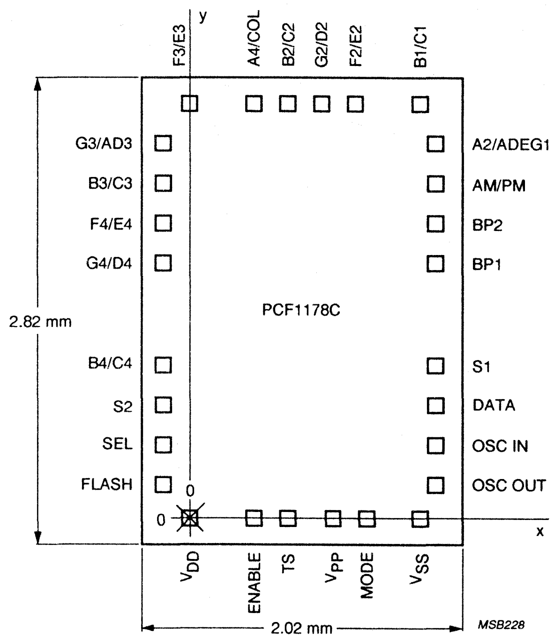
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ±30 x 10^{-6}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	–0.35	–	%/K
		V_{DD} = 4.5 V	–	–16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	μA
C_{EXT}	capacitance	external capacitor	47	–	–	μF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60 x 10^{-6}	110 x 10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1 x 10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
R_O	pull-up/pull-down resistance	MODE	100	300	1000	kΩ
I_{IL}	leakage current	ENABLE, FLASH	–	–	2	μA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD} - 5$ V	70	–	700	μA
		during programming	–	500	–	μA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 μA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 μA	–	–	5	kΩ
LCD						
V_{DC}	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   V_{DD} = 5 V; R max. (12 V – 5 V)/700 μA = 10 kΩ;
   V_{DD} = 5 V; R typ. (12 V – 5 V)/900 μA = 7.8 kΩ (more reserve);
   I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.69 mm².

Bonding pad dimensions: 110 µm x 110 µm.

Chip thickness: 381 ±25 µm.

Fig.8 Bonding pad locations.

Table 2 Bonding pad locations (dimensions in µm).
All x/y coordinates are referenced to the bottom left pad (V_{SS}), see Fig.8.

PAD	X	Y	PAD	X	Y
S1	1490	881	G4/D4	−86	1588
DATA	1490	639	F4/E4	−86	1808
OSC IN	1490	408	B3/C3	−86	2028
OSC OUT	1490	188	G3/AD3	−86	2248
V_{SS}	1352	0	F3/E3	−48	2476
MODE	969	0	A4/COL	352	2476
V_{PP}	770	0	B2/C2	552	2476
TS	506	0	G2/D2	752	2476
ENABLE	306	0	F2/E2	952	2476
V_{DD}	0	0	B1/C1	1352	2476
FLASH	−86	188	A2/ADEG1	1490	2248
SEL	−86	408	AM/PM	1490	2028
S2	−86	628	BP2	1490	1808
B4/C4	−86	848	BP1	1490	1588
chip corner (max. value)	−310	−170			

4-digit duplex LCD car clock PCF1179C

FEATURES

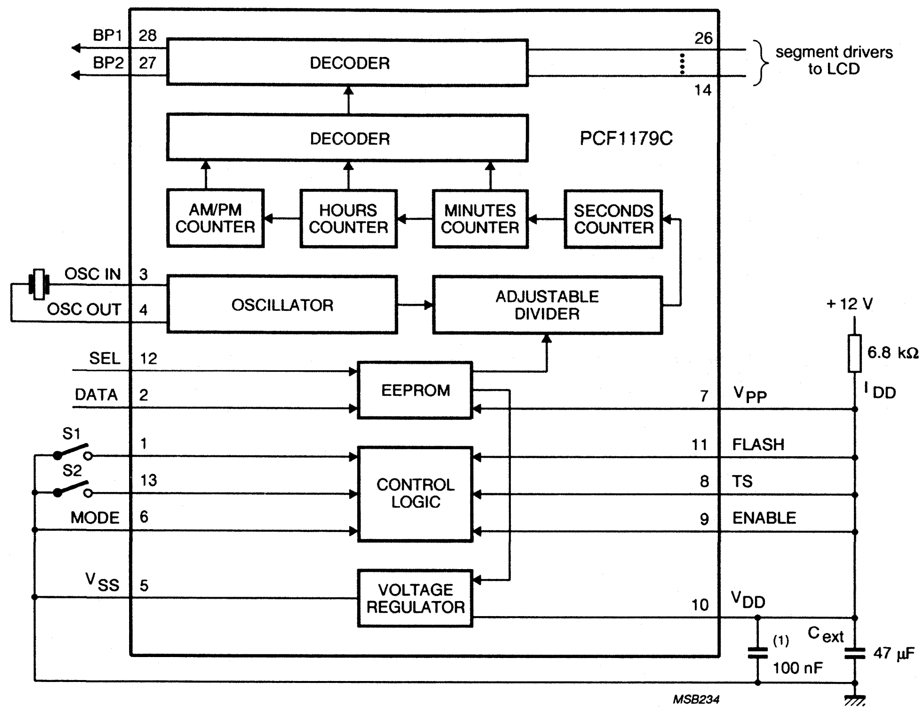
- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 28-lead plastic mini-pack.

GENERAL DESCRIPTION

The PCF1179C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD). Two single-pole, single-throw switches accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF1179CT	28	SO28L	plastic	SOT136A
PCF1179CU	–	uncased chip in tray	–	–
PCF1179CU/10	–	chip-on-film frame carrier (FFC)	–	–



(1) To be mounted close to the IC.

Fig.1 Typical application diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S1	1	hour adjustment input
DATA	2	EEPROM data input
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{SS}	5	negative supply voltage
MODE	6	12/24-hour mode select input
V_{PP}	7	programming voltage input
TS	8	test speed-up mode input
ENABLE	9	enable input (for S1 and S2)
V_{DD}	10	positive supply voltage
FLASH	11	colon option input
SEL	12	EEPROM select input
S2	13	minute adjustment input
B4/C4	14	segment driver
G4/D4	15	segment driver
F4/E4	16	segment driver
B3/C3	17	segment driver
G3/AD3	18	segment driver
F3/E3	19	segment driver
A4/COL	20	segment driver
B2/C2	21	segment driver
G2/D2	22	segment driver
F2/E2	23	segment driver
B1/C1	24	segment driver
A2/ADEG1	25	segment driver
AM/PM	26	segment driver
BP2	27	backplane 2
BP1	28	backplane 1

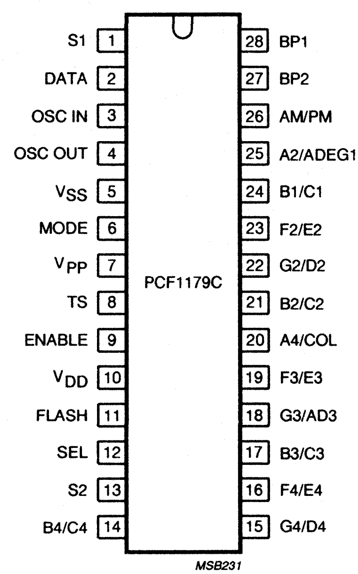


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1:2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.5.

The average voltages across the segments are:

$V_{ON(RMS)} = 0.79\ V_{DD}$

$V_{OFF(RMS)} = 0.35\ V_{DD}$.

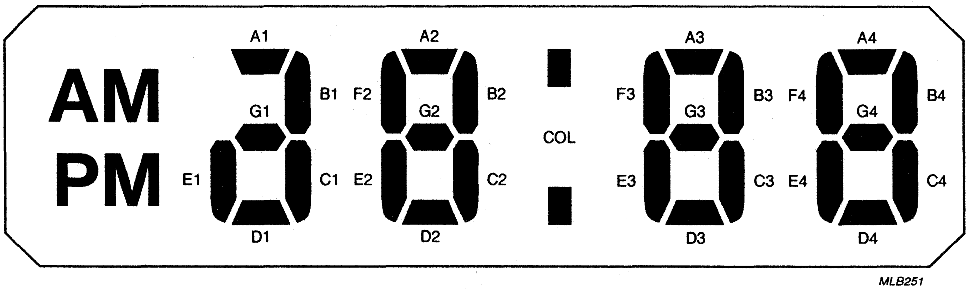


Fig.3 Segment designation of LCD.

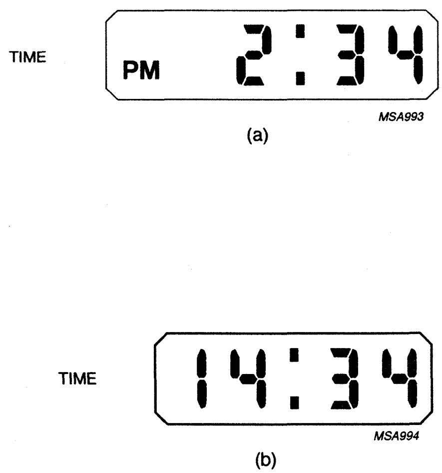


Fig.4 Typical displays; (a) 12-hour mode, (b) 24-hour mode.

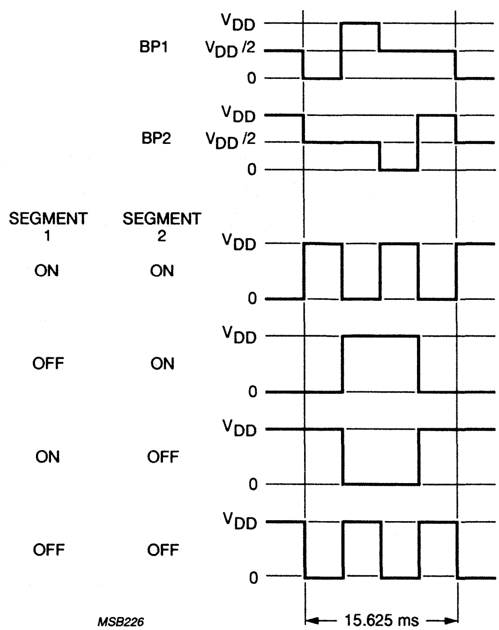


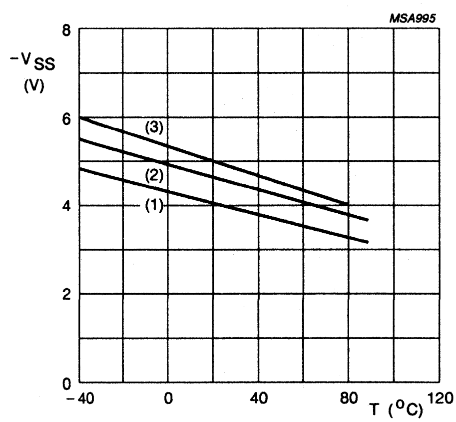
Fig.5 Backplane and output signals.

LCD voltage (Fig.6)

The adjustable voltage regulator controls the supply voltage (see section 'LCD voltage programming') in relation to temperature for good contrast, e.g. when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C

V_{DD} = 5 to 6 V at −40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).

(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).

(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.6 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

MODE connected to V_{DD}:	12-hour mode,	1:00 AM
MODE connected to V_{SS}:	24-hour mode,	0:00
MODE left open-circuit:	24-hour mode,	0:00 or 1:00.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switches S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with four advances per second until S1 is released (auto-increment). An overflow in the hour counter must not have an influence on the minute counter.

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with four advances per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero. An overflow in the minute counter must not have an influence on the hour counter.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.7). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation +60 ppm) by capacitors at the oscillator input and output, a number (n) of 262144 Hz are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.7):

1. Set SEL to V_{SS} and a level of V_{DD} – 5 V to V_{PP}.
2. The quartz-frequency deviation Δf/f is measured and (n) is calculated (see Table 1).
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency.
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and when correct fixed by applying the store pulse t_W.
6. Release SEL and V_{PP}.

Table 1 Time calibration (Δt = 7.63 µs; SEL at V_{SS}).

OSCILLATOR-FREQUENCY DEVIATION Δf/f (ppm)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.633
+7.6	2	15.641
+11.4	3	15.648
.	.	.
.	.	.
.	.	.
+117.8	31	15.861

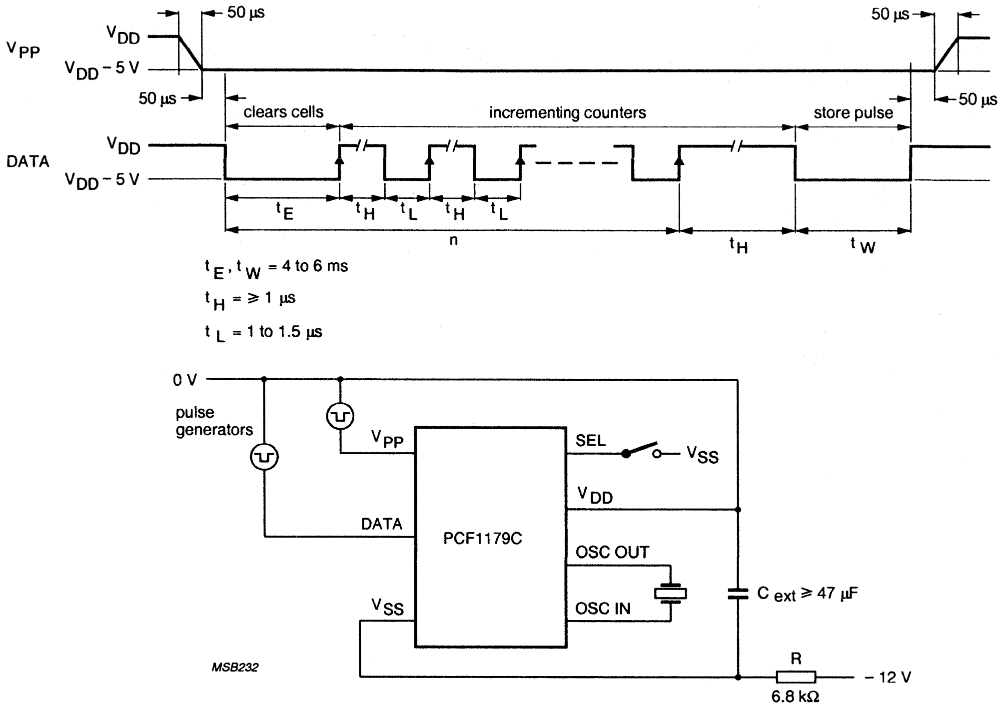


Fig.7 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	voltage range	all pins except V_{PP} and DATA	–0.3	V_{DD}+0.3	V
		pins V_{PP} and DATA	–3	V_{DD}+0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

Handling MOS devices

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

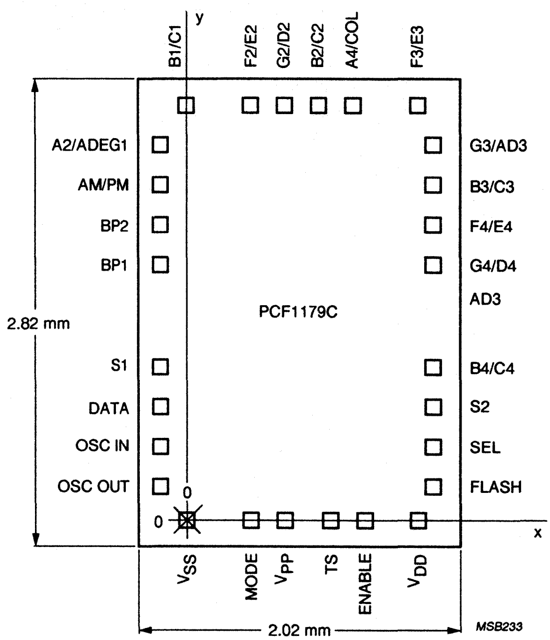
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = ±30 x 10^{-6}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	−0.35	–	%/K
		V_{DD} = 4.5 V	–	−16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	µA
C_{EXT}	capacitance	external capacitor	47	–	–	µF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60 x 10^{-6}	110 x 10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1 x 10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
R_O	pull-up/pull-down resistance	MODE	100	300	1000	kΩ
I_{IL}	leakage current	ENABLE, FLASH	–	–	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD}$ − 5 V	70	–	700	µA
		during programming	–	500	–	µA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 µA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	–	–	5	kΩ
LCD						
V_{DC}	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   V_{DD} = 5 V; R max. (12 V − 5 V)/700 µA = 10 kΩ;
   V_{DD} = 5 V; R typ. (12 V − 5 V)/900 µA = 7.8 kΩ (more reserve);
   I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.69 mm^2.

Bonding pad dimensions: 110 µm x 110 µm.

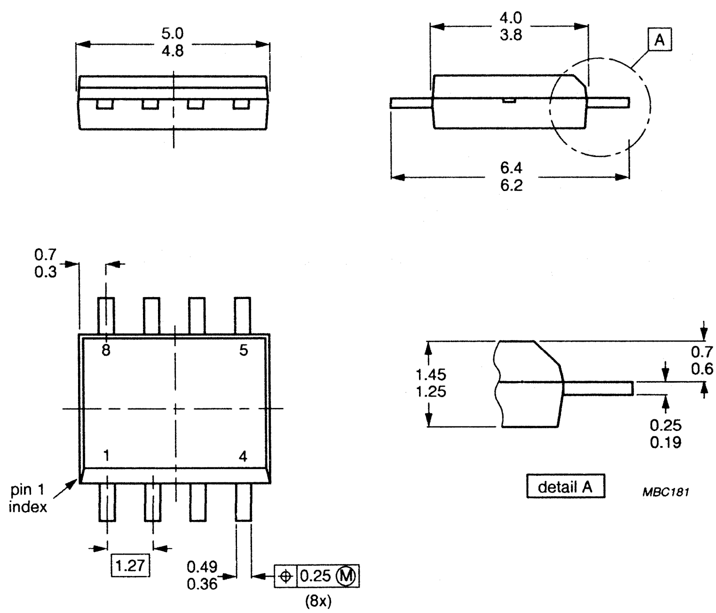
Chip thickness: 381 ±25 µm.

Fig.8 Bonding pad locations.

Table 2 Bonding pad locations (dimensions in µm).
All x/y coordinates are referenced to the bottom left pad (V_{SS}), see Fig.8.

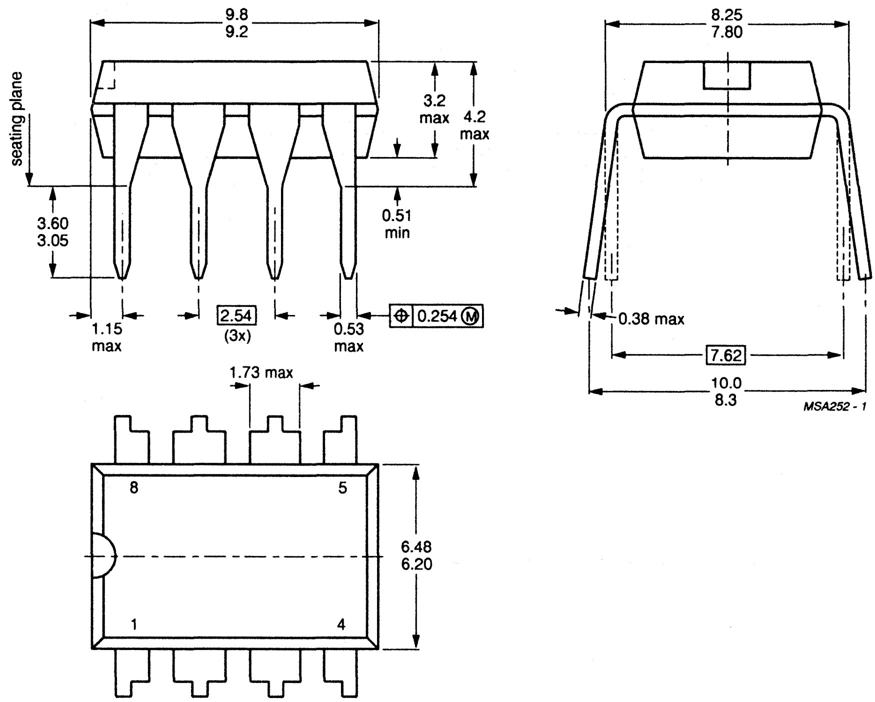
PAD	X	Y	PAD	X	Y
S1	−138	881	G4/D4	1438	1588
DATA	−138	639	F4/E4	1438	1808
OSC IN	−138	408	B3/C3	1438	2028
OSC OUT	−138	188	G3/AD3	1438	2248
V_{SS}	0	0	F3/E3	1400	2476
MODE	383	0	A4/COL	1000	2476
V_{PP}	583	0	B2/C2	800	2476
TS	846	0	G2/D2	600	2476
ENABLE	1046	0	F2/E2	400	2476
V_{DD}	1352	0	B1/C1	0	2476
FLASH	1438	188	A2/ADEG1	−138	2248
SEL	1438	408	AM/PM	−138	2028
S2	1438	628	BP2	−138	1808
B4/C4	1438	848	BP1	−138	1588
chip corner (max. value)	−360	−170			

PACKAGE INFORMATION



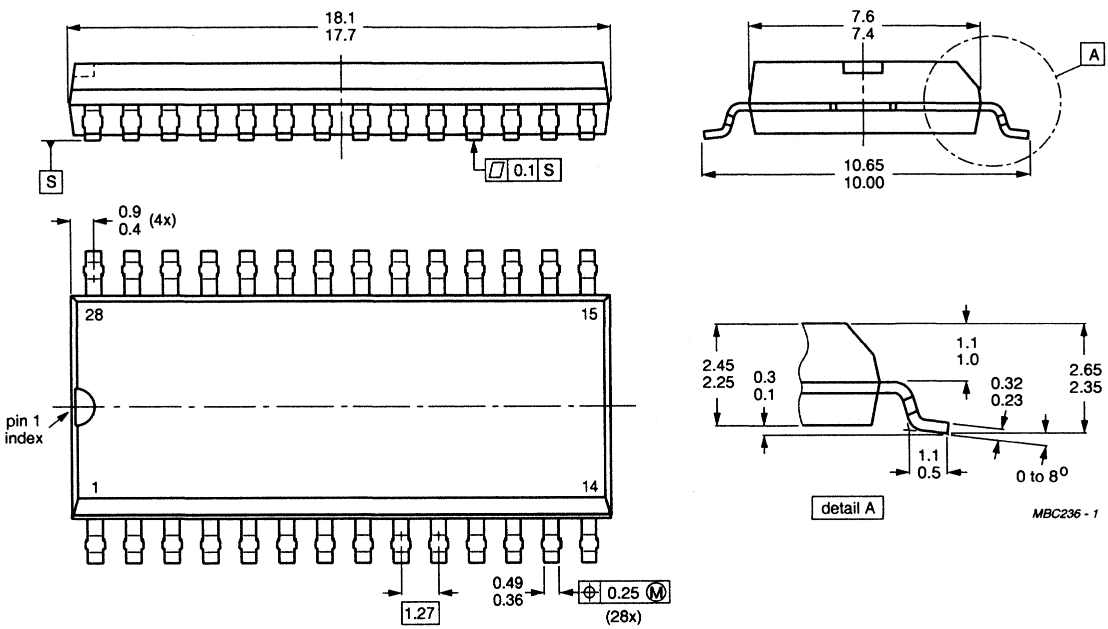
Dimensions in mm.

Fig.1 8-lead mini-pack; plastic (SO8; SOT96C).



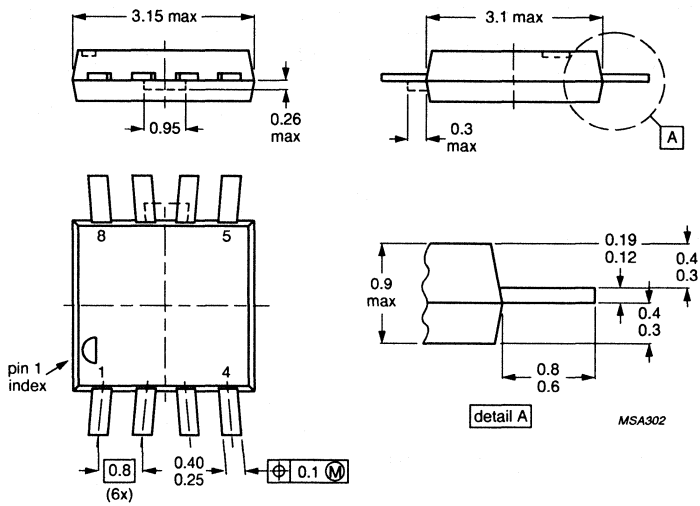
Dimensions in mm.

Fig.2 8-lead dual in-line; plastic (SOT97).



Dimensions in mm.

Fig.3 28-lead mini-pack; plastic (SO28L; SOT136A).



Dimensions in mm.

Fig.4 8-lead micro flat-pack; plastic (SOT144A).

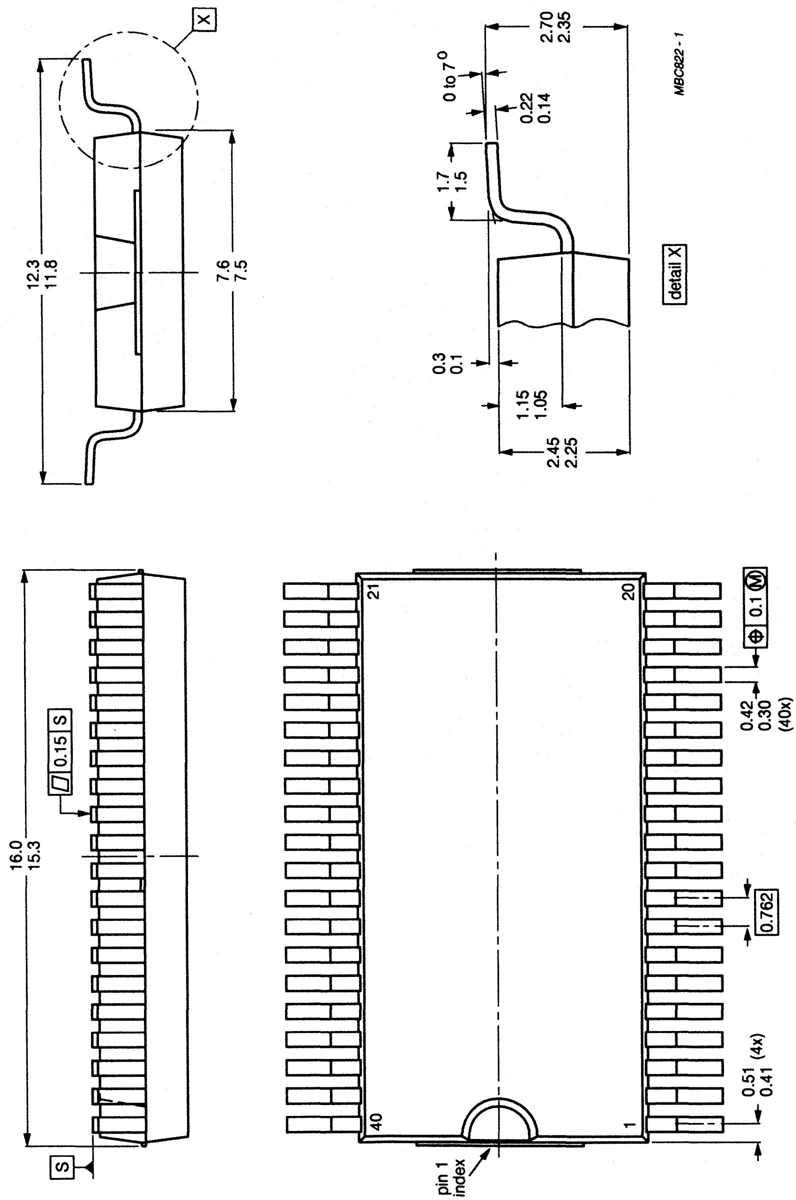


Fig.5 40-lead mini-pack (face down); plastic (VSO40FD; SOT158B).

Dimensions in mm.

SOLDERING

Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

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Data handbook system

DATA HANDBOOK SYSTEM

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Printed in The Netherlands Date of release: 09-'93 9398 652 59011

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